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Commutation Failure Elimination of LCC HVDC Systems Using Thyristor-Based Controllable Capacitors

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***Abstract*—The adverse impacts of commutation failure (CF) of a line-commutated converter (LCC)-based high-voltage direct current (HVdc) system on the connected ac system are becoming more serious for high-power ratings, for example, the development of ultra-HVdc systems. Aiming to solve the problem of CF particularly for higher power/current LCC HVdc systems, this paper proposes a new method, which utilizes a thyristor-based controllable capacitor (TBCC), to eliminate CFs. The topology of the proposed TBCC LCC HVdc and its operating principles are presented. Then, mathematical analysis is carried out for the selection of component parameters. To validate the performance of the proposed method, modified LCC-HVdc and capacitor-commutated converter (CCC)-based HVdc systems based on the modified CIGRE HVdc system are modeled in a real-time digital simulator. Simulation studies for zero impedance single-phase and three-phase faults are carried out, and comparisons are made with both LCC-HVdc and CCC-HVdc systems. Furthermore, voltage and current stress of the TBCC are investigated and power-loss calculations are presented. The results show that the proposed method is able to achieve CF elimination under the most serious faults while the increase of power losses due to the TBCC is small.**

***Index Terms*—Commutation failure, HVDC transmission, HVDC converter, LCC HVDC, thyristor-based controllable capacitor (TBCC), UHVDC.**

I. Introduction

DUE to the geographical separation of energy sources and load centers, Line Commutated Converter (LCC) based High Voltage Direct Current (HVDC) systems have been successfully applied for long distance bulk power transmission thanks to thyristor's superior power handling capability and low operating power losses [1]. However as the further increase of demand and transmission distance, the latest Ultra High Voltage Direct Current (UHVDC) systems are needed for specific projects [2]–[4]. For example in China, a total of 13 UHVDC projects with rated DC voltages of $\pm$800 kV or $\pm$1100 kV have been completed or under construction [5], and the rated transmission power of these projects are between 5 GW to 12 GW. This increased level of power transmission means that the scale of the impact of Commutation Failure (CF) on the AC system is increased. For cases when CF does not cause converter blocking, there will be a more significant reduction of inverter AC system frequency and a higher power shift to the adjacent HVAC lines. For cases when CF causes the blocking of converter stations, the potential economic loss due to the loss of active power transfer is certainly higher. For example, significant generator tripping at rectifier side and the activation of spinning reserves at inverter side are required to compensate the loss of active power transfer. In extreme cases, this cessation of active power transfer can even lead to the blackout of inverter side AC system. Therefore it would be useful to develop new approach to eliminate CF for the latest generation of higher power rating LCC HVDC (e.g., UHVDC).

A number of publications have been dedicated to the mitigation of CF. As discussed in [6], they can be classified into 1) controller modification based methods [7]–[13], and 2) power electronics based methods [14]–[20].

Most of the controller modification based methods are aiming to mitigate successive CFs rather than eliminate CFs. They rely on fast and accurate detection of inverter side faults and are designed to provide a larger commutation margin by advancing inverter firing angles. The main differences between these methods are 1) the way of fault detection, and 2) the way of calculating the firing angle advancement. Reference [8] uses the $abc - \alpha\beta$ transformation for detection of single-phase and three-phase faults, and reference [12] uses a power component fault detection method to improve the detection of single- and three-phase faults. For the calculation of firing angle advancement, [10] and [13] uses fuzzy logic based controllers to determine the extent of firing angle advancement. Reference [7], [9], [11], on the other hand, directly use the inverter AC voltage to calculate the desired firing angle. Improvements in mitigating successive CF can be achieved with these methods but it should be noted that by decreasing the inverter firing angle, inverter reactive power consumption is increased, which leads to further AC voltage drops. Such behavior is unfavorable as a higher AC voltage is needed for a better recovery. Furthermore, as pointed out by [21], CF cannot be eliminated by pure controller modifications.

The most well known main equipment based method in CF mitigation is the Capacitor Commutated Converter (CCC) based

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HVDC [15]. With fixed series capacitor insertions, it can reduce the CF probability but additional valve voltage stress is reported. Also it experiences slower recovery from unbalanced fault [22]. To improve the controllability of inserted capacitors, active series compensations with the help of Insulated Gate Bipolar Transistor (IGBT) are adopted in [6], [17]. However due to the limited current handling capability of IGBTs compared with thyristors, their application in LCC HVDC systems with higher power/current ratings (e.g., UHVDC systems) is limited. Recently an Evolved Capacitor-Commutated-Converter (ECCC) embedded with Anti-Parallel Thyristors based Dual-directional Full-Bridge Module (APT-DFBM) was proposed in [23] to mitigate CF and to improve the dynamic performance of CCC HVDC. The use of thyristors avoids the limitation of current rating from IGBTs and the probability of CF is reduced. A comparison between the proposed method in this paper and the method of ECCC is provided in Section VII. Reference [24], from a different prospective, uses a superconducting fault current limiter to achieve faster recovery by limiting the AC fault current. Another family of power electronics based methods uses shunt connected reactive power compensation devices at the inverter AC side [25], [26]. Those devices are utilized to help the recovery of AC voltage especially during remote fault so that the risk of CF can be reduced. However, they cannot eliminate CFs and the cost of equipment can be significant considering their application in UHVDC projects.

To eliminate CF especially for LCC HVDC systems with higher power/current ratings (e.g., UHVDC systems), this paper proposes an approach using Thyrsitor Based Controllable Capacitor (TBCC). The use of thyristors effectively alleviates the limitation introduced by the present handling capability of IGBTs, and therefore makes it applicable to UHVDC systems. In addition, due to lower power losses of thyristors, the use of TBCC has the extra benefits of lower extra power losses than that using IGBTs.

This paper is organized as follows. In Section II, circuit configuration of TBCC is described. In Section III, the operating principles of TBCC and capacitor voltage control are explained. In Section IV, detailed mathematical analysis is carried out for the selection of component parameters in TBCC. In Section V, simulation results of the proposed system under single- and three-phase faults are presented to validate the effectiveness of the proposed method. Comparisons are made between the proposed TBCC LCC HVDC, LCC-HVDC and CCC-HVDC. In addition, voltage and current stresses of TBCC are investigated. In Section VI, calculations of additional power losses introduced by TBCC are carried out. Finally conclusions are drawn in Section VII.

II. Configuration of the Thyristor Based Controllable Capacitor

Fig. 1 shows the proposed converter configuration at inverter side of the HVDC system. In Fig. 1(a), one 6-pulse thyristor bridge of the 12-pulse inverter is shown where I_d is the DC current, L_s is the DC smoothing reactor, $TY1 - TY6$ are thyristor valves. The complete system is based on the CIGRE HVDC Benchmark model which is a 12-pulse system rated at

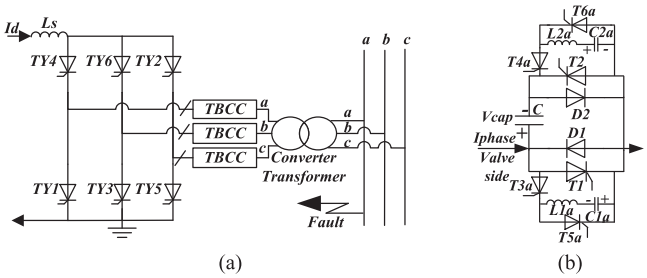

Fig. 1. The proposed converter configuration. (a) Inverter topology with the proposed TBCC (6-pulse); (b) Configuration of the TBCC module.

1000 MW, 500 kV and 2 kA [27]. Fig. 1(b) shows the circuit configuration of one TBCC module. In Fig. 1(b), C is the main capacitor, $T1$ and $T2$ are the main thyristors, and each of them is equipped with an anti-parallel diode, i.e., $D1$ and $D2$, respectively. There are two commutation circuits for turning off the two main thyristors. The first commutation circuit consists of an LC resonant branch, i.e., the branch with inductor $L1a$ and capacitor $C1a$, and two auxiliary thyristors, $T3a$ and $T5a$. The second commutation circuit has the same configuration as the first one with inductor $L2a$ and capacitor $C2a$ forming the resonant branch, and two auxiliary thyristors, $T4a$ and $T6a$. The positive direction of current $I_{\rm phase}$, the positive voltage polarities of the main capacitor $V_{\rm cap}$ and two auxillary capacitors $C1a$ and $C2a$ are also shown in the figure. Each TBCC module can be implemented by a single module or by a number of series connected sub-modules for higher voltage insertions. It should be mentioned that as there is no IGBT, the power handling capability of the TBCC is significantly increased compared with IGBT based modules.

There are two modes of operation for TBCC, i.e., capacitor insertion mode and capacitor bypass mode. For positive I_d, the main capacitor is bypassed or inserted when the current is flowing through $T1$ or through $D2$, respectively. For negative I_d, the main capacitor is bypassed or inserted when the current is flowing through $D1$ or through $T2$, respectively. For both current directions, the positive polarity of the main capacitor is connected to the DC side when inserted. The detailed insertion strategy of TBCC is explained in the next section.

III. Operating Principle and Capacitor Voltage Control

The TBCC in phase C is considered in this section. The steps for initial charging and the detailed operating principles are explained first, and then the method of controlling the capacitor voltage is presented.

A. Initial Charging of TBCC Module

There are five steps for the initial charging of TBCC module. Fig. 2 shows the active conduction path for each step, and the details of each step are described as follows:

Step 1: The main capacitor is charged with positive $I_{\rm phase}$;

Step 2: $T2$ and $T3a$ are fired and $C1a$ is charged by the main capacitor to the polarity shown in Fig. 2. When the voltage across $C1a$ is equal to the main capacitor, the

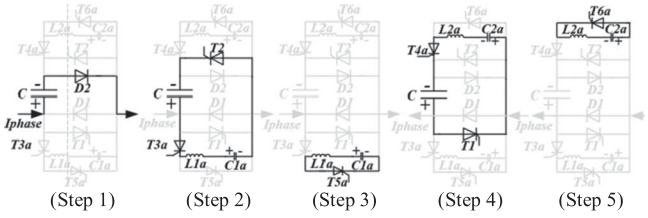

Fig. 2. Active conduction paths of TBCC for initial charging.

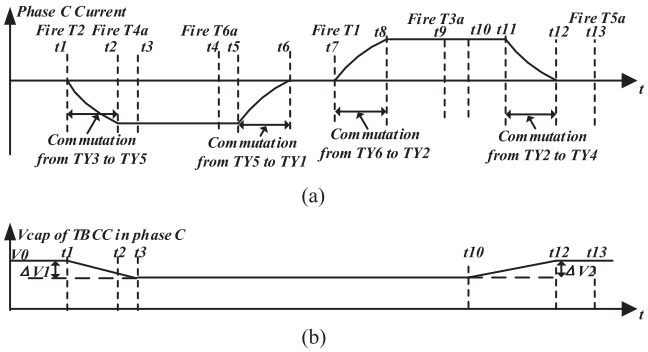

Fig. 3. Operating principle of TBCC in phase C. (a) Phase C current. (b) $V_{\rm cap}$ of TBCC in phase C.

charging is completed and $T2$ and $T3a$ are turned off;

Step 3: $T5a$ is fired, forming a resonant circuit between $C1a, L1a$ and $T5a$. Once resonance is completed, the voltage polarity of $C1a$ is reversed;

Step 4: Similar to step 2, $C2a$ is charged to the polarity shown in Fig. 2 by firing $T1$ and $T4a$;

Step 5: Similar to Step 3, $T6a$ is fired to form a resonant circuit between $C2a, L2a$ and $T6a$. The voltage polarity of $C2a$ is reversed once the resonance is completed.

The voltage of the main capacitor during operation is controlled by the voltage controller described in subsection C of this section. The voltages of $C1a$ and $C2a$ during operation depend on the circuit parameters and the voltage of the main capacitor. Detailed analysis is provided in Section IV.

To explain the operating principles of TBCC, Fig. 3 is used to show the control sequence of TBCC throughout one cycle. Fig. 3(a) shows the phase C current, key timing instants $(t_1$–$t_{13})$ and key firing instants of thyristors. The positive direction of phase C current is defined as flowing out of the converter to the AC system. Fig. 3(b) illustrates the change of main capacitor voltage within the same cycle. The active conduction paths under different stages are shown and highlighted in Fig. 4.

B. Operating Principle

With the voltages of $C1a, C2a$ and C initially charged to the polarity shown in Fig. 1(b), the detailed operating principle can be described as follows with reference to Figs. 3 and 4.

Stage 1 $(t_1$–$t_2)$*:* $T2$ is fired as commutation starts from $TY3$ to $TY5$ at time t_1. The phase current is flowing through $T2$ and the main capacitor C to the DC side, discharging the main capacitor as shown in Fig. 3(b). Due to the insertion orientation, the main capacitor is providing extra commutation voltage;

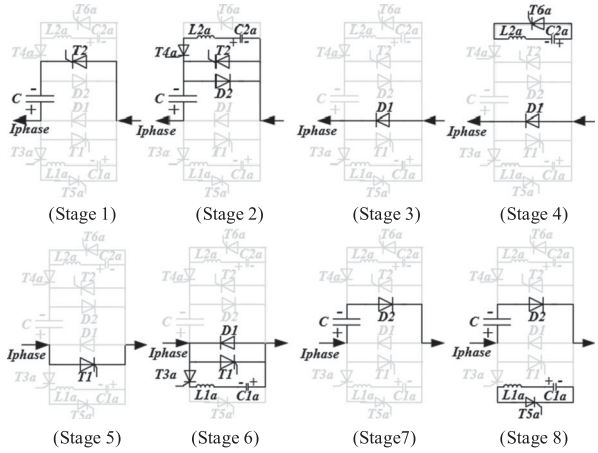

Fig. 4. Conduction path of TBCC in phase C from stage 1 – stage 8.

Stage 2 $(t_2$–$t_3)$*:* $T4a$ is fired once the commutation from $TY3$ to $TY5$ is completed. A resonant circuit is formed between $C2a, L2a, T4a$ and $T2$, and the resonant current through $T2$ is in the opposite direction of the phase current. The voltage of $C2a$ is added across $L2a$ and the resonant current is flowing within the resonant loop, resulting in negligible impact on the harmonic performance of LCC HVDC. $T2$ is turned off when the resonant current is higher than the phase current, and $T4a$ is turned off once the resonant current reaches zero at t_3. At the end of this stage, voltage polarity of $C2a$ is reversed and the main capacitor voltage is further reduced;

Stage 3 $(t_3$–$t_6)$*:* with $T2$ and $T4a$ turned off, phase C current flows through $D1$ into the converter;

Stage 4 (t_4)*:* $T6a$ is fired at t_4, forming another resonant circuit between $C2a, L2a$ and $T6a$. Once resonance is completed, the $C2a$ voltage polarity becomes positive again preparing for the turn-off action in next cycle;

Stage 5 $(t_7$–$t_9)$*:* $T1$ is fired as commutation starts from $TY6$ to $TY2$ at time t_7. The phase current flows through $T1$ to the AC side, and the main capacitor is bypassed;

Stage 6 $(t_9$–$t_{10})$*:* $T3a$ is fired at t_9, forming a resonant circuit between $C1a, L1a, T3a$ and $T1$. $T1$ is turned off when the resonant current is higher than the phase current, and $T3a$ is turned off once resonant current reaches zero at t_{10}. At the end of this stage, voltage polarity of $C1a$ is reversed;

Stage 7 $(t_{10}$–$t_{12})$*:* with $T1$ and $T3a$ turned off, phase current flows through the main capacitor and $D2$ to the AC side, charging the main capacitor. This insertion orientation helps the commutation from $TY2$ to $TY4$ between t_{11} to t_{12}. It needs to be mentioned that the charging time of the main capacitor $(t_{10}$–$t_{12})$ is longer than the discharging time $(t_1$–$t_3)$. This is because the average discharging current (between t_1–t_2) is higher than the charging current $(t_{11}$–$t_{12})$ during commutations (Fig. 3(a)). Therefore additional charging time is required to control the capacitor voltages;

Stage 8 (t_{13})*:* $T5a$ is fired at t_{13}, forming a resonant circuit between $C1a, L1a$ and $T5a$. Similar to stage 4, the voltage polarity of $C1a$ becomes positive again after resonance preparing for the turn-off action in next cycle.

It can be seen from the above description for TBCC in phase C, additional commutation voltages are obtained for two com-

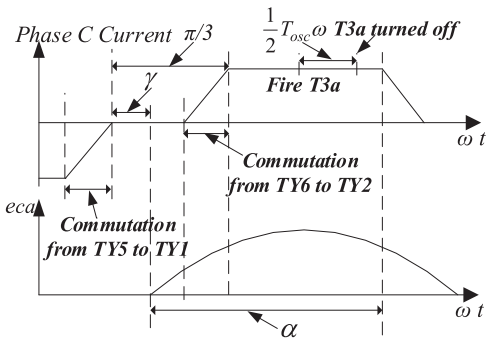

Fig. 5. Derivation of firing angle limits for $T3a$ of TBCC in phase C.

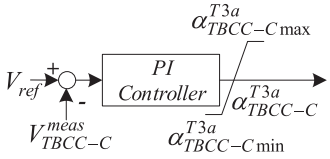

Fig. 6. Capacitor voltage controller for TBCC in phase C.

mutation periods, i.e., from $TY3$ to $TY5$ and from $TY2$ to $TY4$. Similar operating principles are applied to the TBCCs in other two phases, and as a result all six commutation periods are helped by the insertion of TBCCs. With sufficient insertion voltage, the success of commutations can be ensured.

C. Capacitor Voltage Control

The level of main capacitor voltage needs to be controlled to ensure the success of commutations. To illustrate the control strategy, the same TBCC in phase C is taken as an example. Fig. 5 shows the phase C current and the commutation voltage of e_{ca}, and Fig. 6 shows the capacitor voltage controller for TBCC in phase C.

From Fig. 3(b) it can be seen that the main capacitor is discharged during the commutation from $TY3$ to $TY5$, and is charged from the turning-off point of $T3a$ until the end of commutation from $TY2$ to $TY4$. Therefore the level of main capacitor voltage can be controlled by controlling the firing instant of $T3a$. The firing instant (t_9) should be later than t_8, and the turning-off of $T3a\,(t_{10})$ should be earlier than t_{11} so that full DC current is utilized for charging. The actual firing instant for $T3a$ is obtained through a PI controller by minimizing the capacitor voltage error as shown in Fig. 6. In the figure, V_{ref} and V_{TBCC-C}^{meas} are the reference and measured capacitor voltages, $\alpha_{TBCC-C\,\min}^{T3a}$, $\alpha_{TBCC-C\,\max}^{T3a}$ and α_{TBCC-C}^{T3a} are the minimum, maximum and actual firing angles for $T3a$. To calculate the $T3a$ firing angle limits, Fig. 5 is used for the following calculations. With the positive zero-crossing point of e_{ca} as the phase reference, α is the firing angle for $TY4$ and γ is the extinction angle. Then the firing angle limits for $T3a$ can be calculated as

$$\alpha_{TBCC-C\,\min} = \pi/3 - \gamma \tag{1}$$

$$\alpha_{TBCC-C\,\max} = \alpha - 0.5T_{osc}\omega \tag{2}$$

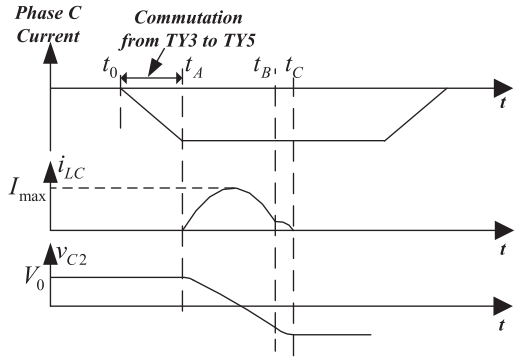

Fig. 7. Dynamics of T2 commutation circuit.

where ω is the system angular frequency and T_{osc} is the resonant period of $C1a$ and $L1a$, which can be calculated as

$$T_{osc} = 2\pi \Big/ \frac{1}{\sqrt{L_1 C_1}} \tag{3}$$

where L_1 and C_1 are the inductance and capacitance of $L1a$ and $C1a$, respectively. If the measured main capacitor voltage is lower than the reference, the firing angle for $T3a$ will be advanced to charge up the voltage, otherwise it is delayed to provide less charging. In this way the main capacitor voltage can be controlled at its reference level to provide sufficient commutation voltage. The balancing of voltages between sub-modules is achieved by applying the controller shown in Fig. 6 to each sub-module. In this way the balancing of capacitor voltages are automatically achieved, and no additional control coordination is required. The same control strategy is applied to TBCC in other phases except the use of different phase references.

IV. Theoretical Analysis and Parameter Selections

For satisfactory operation of TBCC, the following component parameters need to be determined: 1) capacitance and inductance of the commutation circuits, i.e., C_1, C_2, L_1 and L_2; 2) capacitance and voltage reference of the main capacitor. In this section, detailed mathematical analysis is carried out, and based on that component parameters are selected.

A. Dynamics of the Commutation Circuits

As the behavior of commutation circuits are the same, only one is considered here. Fig. 7 shows the electrical variables associated with the commutation circuit for $T2$ of TBCC in phase C. In Fig. 7, t_0 is the start of commutation from $TY3$ to $TY5$, t_A is the end of commutation, t_B is the time instant when $D2$ is turned off, t_C is the time instant when $T4a$ is turned off, i_{LC} is the resonant current, $I_{\max}$ is the maximum resonant current and V_0 is the voltage of $C2a$ before t_A.

The behavior of commutation circuit can be divided into two periods. Period 1 $(t_A$–$t_B)$ is the period between the firing of $T4a$ and the turning-off of $D2$. Period 2 $(t_B$–$t_C)$ is the period between the turning-off of $D2$ and the turning-off of $T4a$. The equivalent circuits for both periods are shown in Fig. 8. According to Fig. 8(a), the dynamic equations for period 1 can be

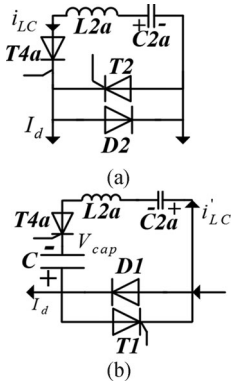

Fig. 8. Equivalent circuits. (a) Period 1 (t_A–t_B). (b) Period 2 (t_B–t_C).

written as

$$-v_c(t)+L_2\frac{di_{LC}(t)}{dt}+R_{T4a}i_{LC}(t)-(I_d-i_{LC}(t))R_{D2}=0 \tag{4}$$

$$i_{LC}(t)=-C_2\frac{dv_c(t)}{dt} \tag{5}$$

with the initial conditions of

$$v_c(t_A)=V_0 \tag{6}$$

$$i_{LC}(t_A)=-C_2\frac{dv_c(t)}{dt}\bigg|_{t=t_A}=0 \tag{7}$$

where I_d is the DC current, v_c is the voltage of $C2a$, R_{T4a} is the resistance of $T4a$ and R_{D2} is the resistance of $D2$. As $T2$ is turned off shortly after the firing of $T4a$, its resistance is not considered. Solve (4)–(5) with the initial conditions of (6)–(7) and take t_A as the time reference, $C2a$ voltage is obtained as

$$v_c(t)=K_1e^{-\frac{a}{2}t}\cos\omega_n t+K_2e^{-\frac{a}{2}t}\sin\omega_n t-I_dR_{D2} \tag{8}$$

where

$$a=R_{T4a}+R_{D2}/L_2;\ b=1/L_2C_2 \tag{9}$$

$$K_1=V_0+I_dR_{D2} \tag{10}$$

$$K_2=aK_1/2\omega_n \tag{11}$$

$$\omega_n=\sqrt{b-\left(a^2/4\right)} \tag{12}$$

Substitute (8) into (5), the resonant current is obtained as

$$i_{LC}(t)=-C_2\frac{dv_c(t)}{dt}=\frac{K_1}{\omega_nL_2}e^{-\frac{a}{2}t}\sin\omega_n t \tag{13}$$

As the resonant period is short and the loop resistances are small, the resonant current can be approximated by

$$i_{LC}(t)\approx V_0\sin\omega_n t\Big/\frac{L_2}{\sqrt{L_2C_2}}=I_{\max}\sin\omega_n t \tag{14}$$

For period 2, with reference to Fig. 8(b), the dynamic equations and the associated initial conditions are

$$v'_c(t)+L_2\frac{di'_{LC}(t)}{dt}-V_{\rm cap}=0 \tag{15}$$

$$i'_{LC}(t)=C_2\frac{dv'_c(t)}{dt} \tag{16}$$

$$i'_{LC}(t_B)=I_d=C_2\frac{dv'_c(t)}{dt} \tag{17}$$

$$v'_c(t_B)=V'_0 \tag{18}$$

where the superscripts denote the variables for period 2. The value of $V_{\rm cap}$ is considered to be constant in period 2 as the main capacitance is much larger than the auxiliary capacitance. As period 2 is very short, resistances in the circuit are neglected. Considering (16)–(17) and take t_B as time reference, $C2a$ s voltage and resonant current can be calculated:

$$v'_c(t)=K'_1\cos\omega'_nt+K'_2\sin\omega'_nt+V_{\rm cap} \tag{19}$$

$$i'_{LC}(t)=-C_2K'_1\omega'_n\sin\omega'_nt+I_d\cos\omega'_nt \tag{20}$$

where

$$K'_1=V'_0-V_{\rm cap} \tag{21}$$

$$\omega'_n=1\Big/\sqrt{L_2C_2} \tag{22}$$

$$K'_2=I_d/\omega'_nC_2 \tag{23}$$

Considering the resonant current becomes zero at t_C, the $C2a$ voltage at t_C can be calculated as

$$v'_c(t_C)=\sqrt{{K'_1}^2+{K'_2}^2}+V_{\rm cap} \tag{24}$$

It can be seen from (24) that the voltage of $C2a$ is dependent on the main capacitor voltage at t_C. The phase current $I_{\rm phase}$ is charging $C2a$ between t_B and t_C to compensate for the losses of resonant circuit. Therefore the voltage of $C2a$ will not decrease due to the losses in the resonant circuit as long as the main capacitor voltage is controlled.

B. Parameter Selection for Main Capacitor

The capacitance value for the main capacitor is chosen so that the variation of its voltage is not significant after each discharge/charge period. According to the analysis carried out in [6], considering the increase of DC current, the value of 880 μF is chosen for simulation study. For the required voltage level of the main capacitor, a value of more than 200 kV should be required [6]. However in the proposed method as the capacitor modules are taking part in the formation of DC voltage, and an early insertion before the start of commutation reduces the increase of DC fault current, the required voltage insertion is less. The value of the main capacitor voltage reference is obtained as 200 kV from simulation studies.

C. Parameter Selection for Commutation Circuits

Two requirements are considered for the selection of commutation circuit parameters. The first requirement is that the maximum resonant current $I_{\max}$ should be higher than the maximum

DC fault current. In this paper, $I_{\max}$ of 10 kA is chosen as an example. It should be noted that modern thyristors have no problem handling such level of current given the short resonant period. The average and RMS value of resonant current are well within the allowable range of thyristors which are demonstrated in Section VI. The second requirement is that the available charging time of the main capacitor should be sufficiently longer than the discharging time. With reference to Figs. 3(a) and 5, the available discharging and charging time of the main capacitor outside commutation period are given as

$$T_{\text{discharge}} = T_{osc}/2 \tag{25}$$

$$T_{\text{charge}} = (2\pi/3 - \mu)/\omega - T_{osc}/2 \tag{26}$$

where μ is the overlap angle. The second requirement can then be expressed as

$$T_{\text{charge}} \geq k \times T_{\text{discharge}} \tag{27}$$

where k is the margin factor and is chosen as 1.3 for sufficient charging time. Simplify (27) by substituting (25) and (26) gives

$$\sqrt{L_2 C_2} \leq (2\pi/3 - \mu)/(\pi\omega(k+1)) \tag{28}$$

To find the required range of L_2 and C_2, additional relationship between them is required. This can be obtained by analyzing the energy loss and voltage drop of $C2a$ within one cycle. The main energy loss of commutation circuit for $T2$ is coming from the resonant circuit as shown in Fig. 8 between t_A and t_B, and a minor part from the resonant circuit of $T6a - L2a - C2a$ after the firing of $T6a$.

The total energy loss in one AC cycle can be calculated as

$$E_{\text{loss}} = \left(I_{\max}\Big/\sqrt{2}\right)^2 \times (\pi/\omega_n') \times (R_{T4a} + R_{D2} + R_{T6a}) \tag{29}$$

where R_{T6a} is the resistance of $T6a$. Define ΔV as the associated voltage drop of $C2a$, E_{loss} can also be expressed as

$$E_{\text{loss}} = C_2(V_0 + \Delta V)^2\Big/2 - C_2 V_0^2/2 \approx C_2 V_0 \Delta V \tag{30}$$

Now $C2a$ voltage at t_B can be expressed as

$$v_c'(t_B) = V_0' = V_0 - m\Delta V \tag{31}$$

where

$$m = (R_{T4a} + R_{D2})/(R_{T4a} + R_{D2} + R_{T6a}) \tag{32}$$

Under steady-state, the losses should be compensated by the charging action between t_B and t_C, i.e.,

$$v_c'(t_C) = V_0 + \Delta V \tag{33}$$

Now by substituting (31) and (33) into (24), the equation for solving V_0 can be obtained as

$$\left(\frac{I_d}{\mathrm{I}_{\max}}\right)^2 V_0^2 - 2\Delta V(m+1)(V_0 - V_{\text{cap}}) + (m^2-1)\Delta V^2 = 0 \tag{34}$$

With the specified $I_{\max}$, V_0 can be calculated using (34), and the relationship between L_2 and C_2 is obtained by considering

$$I_{\max} = V_0\sqrt{C_2/L_2} \tag{35}$$

The ranges of values for L_2 and C_2 can be calculated by solving (35) and (28) together:

$$L_2 \leq 0.005 \text{ H} \tag{36}$$

$$C_2 \leq 130\ \mu\text{F} \tag{37}$$

The overlap angle of 15 degrees, equivalent resistances of 0.1 ohm and the m of 0.6 are used for the above calculation. As an example, 40 kV of V_{cap} is chosen which indicates five such modules are needed to provide the 200 kV insertion.

V. Simulation Results

A. Fault Dynamics of 500 kV/3 kA HVDC System

To validate the effectiveness of the proposed method, simulation results for zero impedance single-phase and three-phase faults are presented, and comparisons are made with LCC-HVDC and CCC-HVDC. All three systems are established based on the CIGRE benchmark model with their rated DC current increased to 3 kA. The sizes of capacitor banks for the LCC-HVDC and the proposed system are increased to accommodate the increase of reactive power consumption. For CCC-HVDC, the capacitor banks and filters are providing 15% of the reactive power [16]. The series capacitance of 90 μF is selected for CCC-HVDC so that the average commutation voltage being provided during commutation is similar to that of the proposed method. The inductances of 0.005 H and capacitances of 130 μF are chosen for all commutation circuits.

Fig. 9 shows the simulation results of 60 ms zero impedance phase C to ground fault at inverter side. When fault is initiated at 0.08 s, phase C voltage drops to zero as shown in Fig. 9(a). It can be seen from Fig. 9(c) that there is no CF in the proposed system, while CF can be observed in both CCC-HVDC and LCC-HVDC systems from Fig. 9(d) and (e). As a result, the DC voltage of the proposed system does not drop to zero (Fig. 9(b)), enabling the system to transmit active power during the fault period (Fig. 9(f)). On the other hand, the DC voltages drop to zero for CCC and LCC as shown in Fig. 9(b) and hence no active power can be transmitted (Fig. 9(f)). Fig. 9(g) shows that the insertion voltages from TBCC are well controlled.

Fig. 10 shows the simulation results of 110 ms zero impedance three-phase fault at inverter side. When fault is initiated at 0.13 s, three-phase voltages drop to zero as shown in Fig. 10(a). However, as illustrated in Fig. 10(c), no CF occurs in the proposed method. For CCC-HVDC shown in Fig. 10(d), first few commutations are successful due to additional commutation voltage from fixed capacitors but CFs can be observed when capacitor voltage drops. For LCC-HVDC, CF occurs once the fault is triggered (Fig. 10(e)). DC voltage and active power drop to zero in all three systems but the proposed system achieves a faster recovery as shown in Fig. 10(b) and (f). Also from Fig. 10(b) and (f), it can be seen that CCC-HVDC recovers faster than LCC-HVDC. This is due to the less reactive power absorption of CCC-HVDC during recovery. Again the insertion voltage is well controlled during fault as shown in Fig. 10(g). Fig. 10(h) shows the zoomed-in plot of capacitor voltages between 0.25 s and 0.3 s. The same key timing instants for phase C as those

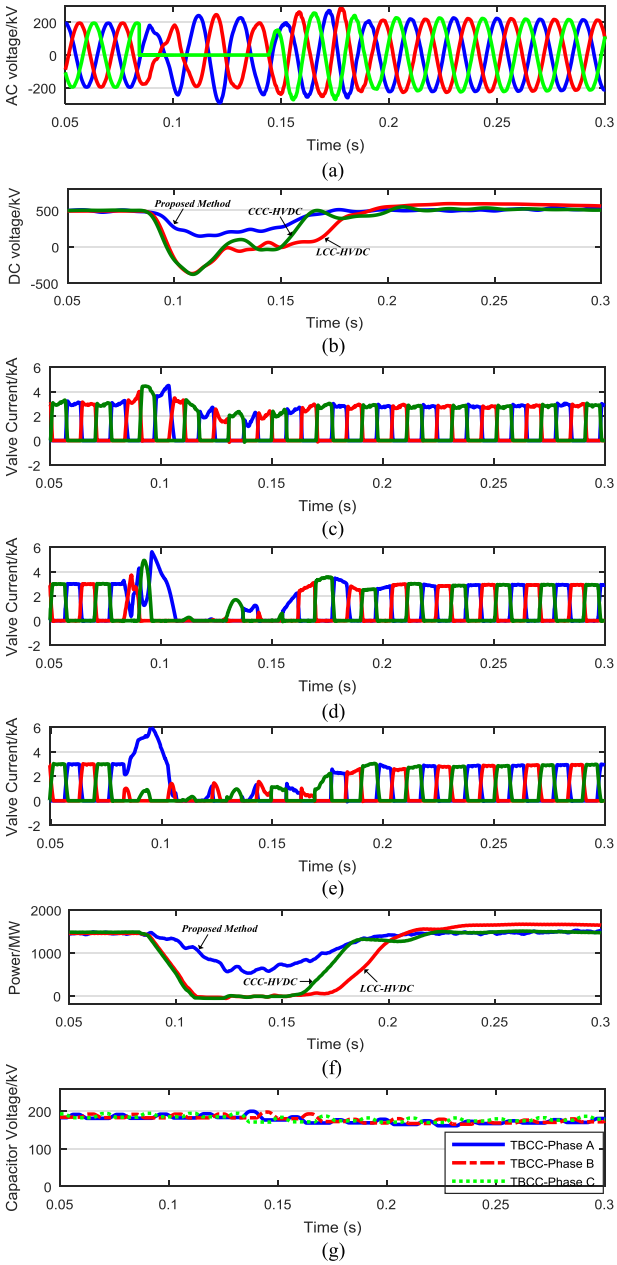

Fig. 9. System response with zero impedance single-phase fault. (a) Inverter AC voltage. (b) DC voltage. (c) Valve currents of the proposed TBCC approach. (d) Valve currents of CCC-HVDC. (e) Valve currents of LCC-HVDC. (f) DC power. (g) Total insertion voltages of TBCCs.

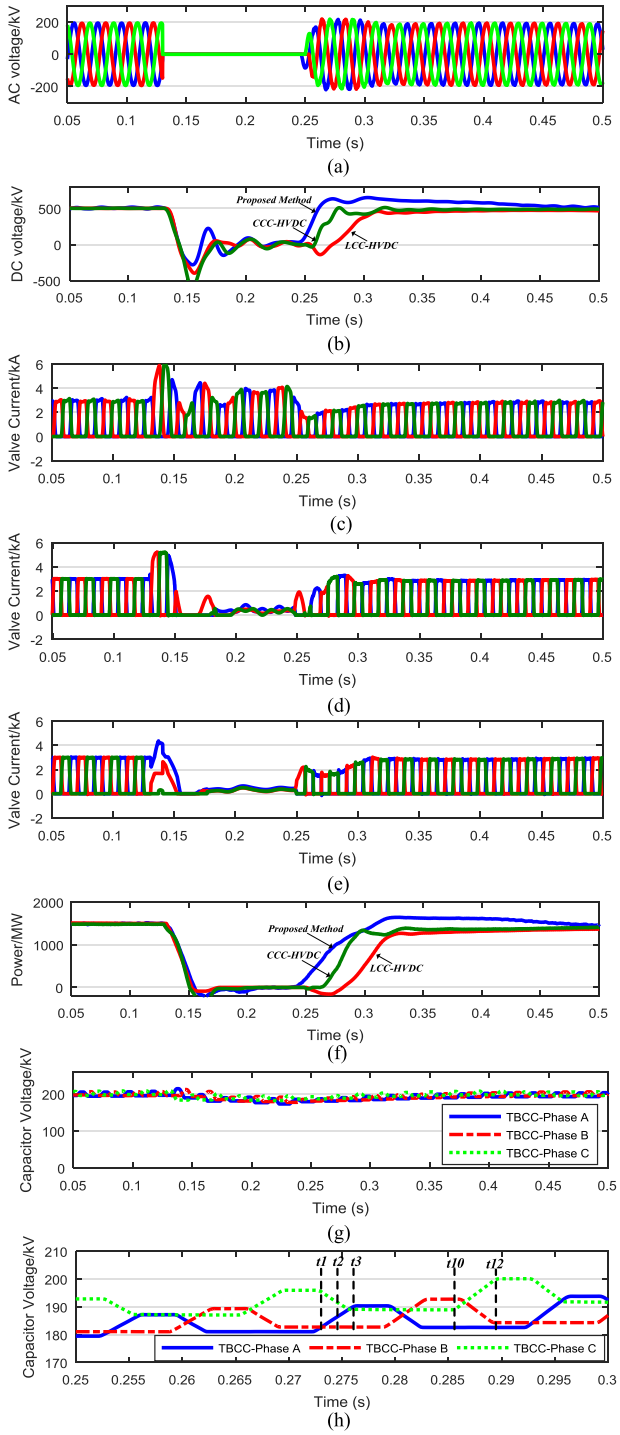

Fig. 10. System response with zero impedance three-phase fault. (a) Inverter AC voltage. (b) DC voltage. (c) Valve currents of the proposed TBCC approach. (d) Valve currents of CCC-HVDC. (e) Valve currents of LCC-HVDC. (f) DC power. (g) Total insertion voltages from TBCCs. (h) Zoomed-in plot of capacitor voltages in Fig. 10(g).

shown in Fig. 3(b) are included. It can be seen that the phase C capacitor voltage is decreased for commutation from $TY3$ to $TY5\,(t_1 - t_2)$, and is further decreased until the capacitor is bypassed (t_3). As the capacitor voltage is lower than the reference (because of the fault), it is inserted into the circuit at t_{10} to charge up the voltage until commutation from $TY2$ to $TY4$ is completed (t_{12}).

B. Fault Dynamics With Larger AC Systems

To demonstrate the capability of the proposed method with larger AC systems, the system as shown in Fig. 11 is

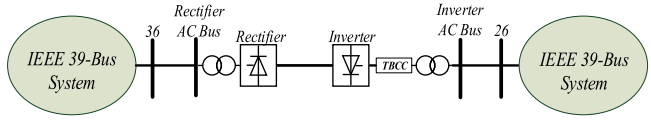

Fig. 11. Network configuration with larger AC systems.

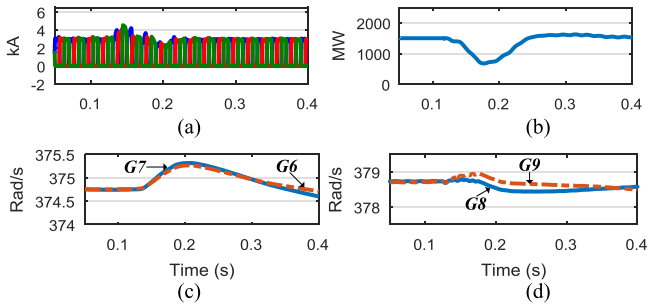

Fig. 12. Simulation results of zero impedance single-phase fault. (a) Valve currents. (b) DC active power. (c) Rotor speed at rectifier AC system. (d) Rotor speeds at inverter AC system.

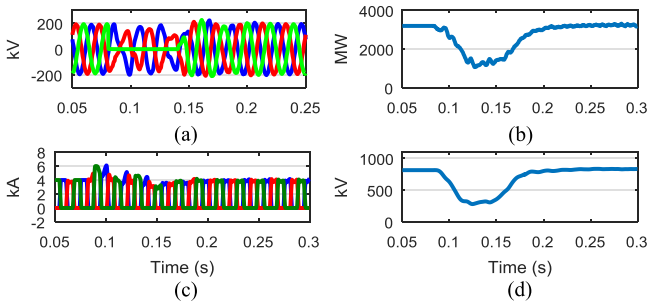

Fig. 13. System response with zero impedance single-phase fault. (a) Inverter AC voltage. (b) DC active power. (c) Valve Currents. (d) DC voltage.

established in RTDS where the IEEE 39-Bus system [28] is used to represent the AC systems of both rectifier and inverter sides. The synchronous generators, excitation systems and governor systems are modelled in detail. The rectifier side is connected to bus 36 and the inverter side is connected to bus 26 (the full single-line diagram is not shown here due to the page limit and the same bus numbers as those in [28] are used).

Fig. 12 shows the simulation results of the system under 60 ms zero impedance single-phase fault at inverter AC bus. It can be seen from Fig. 12(a) that CF does not occur and the HVDC system is able to transmit active power during fault (Fig. 12(b)). Fig. 12(c) shows the rotor speeds of the synchronous generators (G6 and G7) that are electrically close to bus 36 and Fig. 12(d) shows the rotor speeds of the synchronous generators (G8 and G9) that are electrically close to bus 26 (the same numbering system for generator as those in [28] are used). It can be seen that the rotor speeds at rectifier side are increased due to the drop of active power transfer. The inverter side rotor speeds are increased as fault happens due to the drop of bus voltages and are then decreased due to the decrease of active power from HVDC.

C. Fault Dynamics of 800 kV/4 kA UHVDC System

To further demonstrate the capability of the proposed method, a UHVDC system rated at 800kV/4kA is established based on the CIGRE benchmark system. Due to the increased rating of UHVDC system, the required insertion voltage level from TBCC is increased, and the value of 250 kV is obtained from simulation studies. Figs. 13–15 show the simulation results of the system under single-phase fault (phase C to ground), three-phase fault and double-phase to ground fault (phase A and

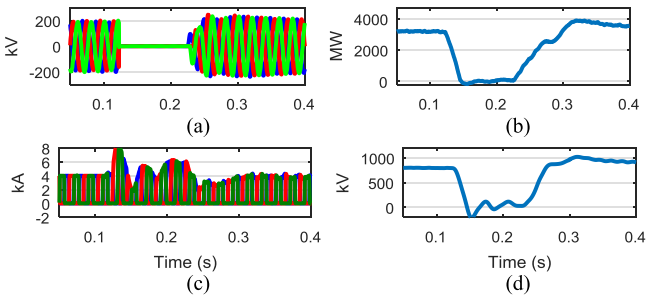

Fig. 14. System response with zero impedance three-phase fault. (a) Inverter AC voltage. (b) DC active power. (c) Valve currents. (d) DC voltage.

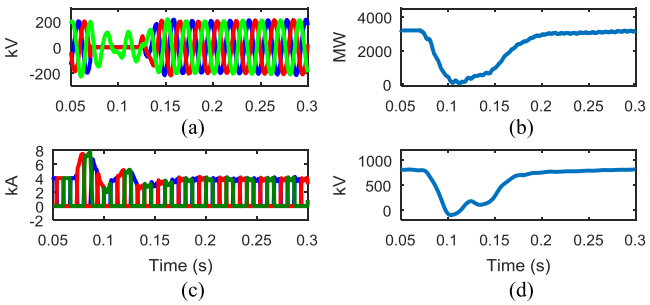

Fig. 15. System response with zero impedance double-phase to ground fault. (a) Inverter AC voltage. (b) DC active power. (c) Valve currents. (d) DC voltage.

phase B to ground), respectively. For single-phase fault, it can be seen from Fig. 13(a) that phase C voltage (green) is dropped to zero during the fault, but no CF is observed as shown in Fig. 13(c). As a result, the UHVDC system is able to maintain a non-zero DC voltage (Fig. 13(d)) and transmit active power during the fault (Fig. 13(b)). For three-phase fault, the three-phase voltages are dropped zero as shown in Fig. 14(a), but no CF occurs due to the insertion of TBCC modules (Fig. 14(c)). Similar to Fig. 10, the DC voltage drops to zero (Fig. 14(d)) and there is no active power transfer during the fault (Fig. 14(b)). For double-phase to ground fault, the phase A and phase B voltages are dropped to zero as illustrated in Fig. 15(a). As shown in Fig. 15(c), no CF occurs during the fault period. The DC voltage drops to zero after fault is initiated and then recovers due to the controller actions (Fig. 15(d)). A certain level of active power can be transmitted during the fault as shown in Fig. 15(b).

D. TBCC Performance

To better illustrate the performance of TBCC in detail, Fig. 16 shows the detailed waveforms within TBCC of phase C. The same time instants as those shown in Figs. 3 and 7 are used, and the capacitor reference voltage of 40 kV is considered. The currents flowing through $ITY2$ and $ITY5$ are shown in both Fig. 16(a) and (b) for time references. The firing sequences and the change of main capacitor voltage shown in Fig. 16(a) are the same as those described in Section III and are not repeated here. It can be seen from Fig. 16(a) that the peak resonant current for turning off $T1$ and $T2$ is about 10 kA, hence both $T1$ and $T2$ are turned off shortly after the firing of $T4a$ and $T3a$. The bottom plot of Fig. 16(a) shows the current through the main capacitor. It is the same as the current through $TY5$ after $T2$ is fired at t_1, and the current through $TY2$ when $T3a$ is turned off

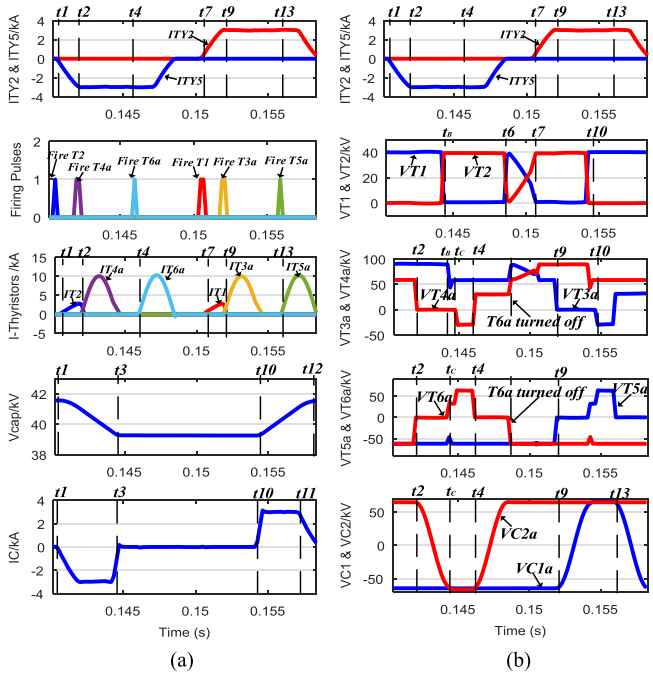

Fig. 16. Performance of TBCC. (a) Thyristor firing pulses & currents, and main capacitor voltage and current; (b) Thyristor forward voltages and voltage across $C1a$ and $C2a$.

at t_{10}. It should also be mentioned that the firing of $T5a$ before the turning off of $TY2$ is due to the early firing of $T3a$.

Fig. 16(b) shows the voltages of $T1-T2, T3a-T6a$, and $C1a$ and $C2a$. From Fig. 16(b), it can be seen that once $T4a$ is fired at t_2, the voltages across $T4a$ and $T6a$ drops to zero. The voltage of $C2a$ starts to decrease due to resonance. At time t_B, when the oscillation current is equal to the DC current, $T2$ and $D2$ are turned off so $T2a$ voltage is equal to the main capacitor voltage, and the voltage of $C1a$ is added across $T3a$. Next when $T4a$ is turned off at t_C, its voltage is equal to the voltage difference between $C2a$ and the main capacitor. At the same time $T6a$ is experiencing the voltage of the main capacitor. The voltage of $C2a$ is kept unchanged as resonance is completed. At $t_4, T6a$ is fired and starts to conduct, so $T6a$ voltage drops to zero and $T4a$ is experiencing the main capacitor voltage. The voltage of $C2a$ starts to reverse as resonance continues. At the time instant when $T6a$ is turned off as highlighted in Fig. 16(b), $C2a$ voltage is reversed and is added across $T6a$. The voltage of $T4a$ is equal to the sum of main capacitor voltage and $C2a$ voltage. $T3a$ is experiencing the voltage of $C1a$ as $T1$ is conducting. At t_6 when commutation from $TY5$ to $TY1$ is completed, $T2$ voltage drops and is increased again to the main capacitor voltage when $T1$ is fired at t_7. The voltage of $T1$ is the difference of the main capacitor voltage and the voltage across $T2$. At t_9 when $T3a$ is fired, its voltage and the voltage of $T5a$ drop to zero. The voltage of $C1a$ starts to reverse because of resonance. When $T1$ and $D1$ are turned off shortly before $t_{10}, C2a$ voltage is added across $T4a$, and $T2$ voltage drops to zero. The change of voltage across $T5a$ is the same as the voltage across $T6a$ in the first half cycle and is not repeated here. When $T5a$ is fired at t_{13}, the voltage of $C1a$ starts to reverse due to resonance. From the above analysis it can be seen that the highest valve voltage appears on $T4a$, and is equal to the sum of main capacitor voltage and $C2a$ voltage. A series connection of multiple thyristors can be utilized to make sure the forward voltage across each thyristor is within allowable range. It can also be seen that the voltage imposed on TBCC module is mainly determined by the voltage level of the main capacitor. Therefore under fault conditions, the voltage imposed on the TBCC will be decreased with decreased main capacitor voltage (Figs. 9(g) and 10(g)).

TABLE I
COMPARISON BETWEEN PROPOSED AND BENCHMARK SYSTEMS

	Proposed System		Benchmark System	
	V (%)	I (%)	V (%)	I (%)
THD	1.21%	0.80%	0.96%	0.52%

TABLE II
CONDUCTION DETAILS OF PHASE C SUB-MODULE

Conduction or Commutation Period	Component	Time Duration	Average/RMS Current (kA)
$TY3$ to $TY5$	$T2$	μ/ω	0.0625/0.354
$TY5$ to $TY1$	$D1$	μ/ω	0.0625/0.354
$TY6$ to $TY2$	$T1$	μ/ω	0.0625/0.354
$TY2$ to $TY4$	$D2$	μ/ω	0.0625/0.354
Turning-off of $T2$	$T4a\&D2$	$0.5\mathrm{T_{osc}}$	0.8062/2.52
Turning-off of $T1$	$T3a\&D1$	$0.5\mathrm{T_{osc}}$	0.8062/2.52
$TY5$ ($T4a$ is off)	$D1$	$(120^0-\mu-0.5\mathrm{T_{osc}})/\omega$	0.4951/1.22
$TY2$ (before $T3a$ is fired)	$T1$	$\Delta\mathrm{t}$	0.075/0.47
$TY2$ ($T3a$ is off)	$D2$	$(120^0-\mu-0.5\mathrm{T_{osc}}-\Delta\mathrm{t})/\omega$	0.4201/1.12
Reverse $C1a$ voltage	$T5a$	$0.5\mathrm{T_{osc}}$	0.8062/2.52
Reverse $C2a$ voltage	$T6a$	$0.5\mathrm{T_{osc}}$	0.8062/2.52

In terms of harmonic impact from TBCC, Table I shows the comparisons of THDs for AC voltage and current between the benchmark system and the proposed method. It can be seen that the THDs are increased due to the capacitor insertions but are still within acceptable limits.

VI. ESTIMATION OF POWER LOSS

The increase of power losses due to additional TBCCs is estimated in this section. As an example, the Phase Controlled Thyristor (PCT) with a rated voltage of 7.2 kV and rated average on-state current of 4840 A [29], and the power diode of [30] are used for calculation. Using the same design as described before, 5 sub-modules are required for each phase and 30 sub-modules are required for the 12-pulse inverter.

To calculate the power losses from each sub-module, Table II shows the conduction period and the corresponding device of one sub-module from Phase C with reference to Figs. 2 and 3. By using the overlap angle of 15° and Δt of 0.5 ms, the

associated average and RMS currents are calculated and shown in the table (valve currents during commutations are assumed to be linear for simplicity). These values are then used to calculate the on-state power utilizing the equation [31]:

$$P = V_0 \times I_{av} + r \times I_{\rm rms}^2 \tag{38}$$

where V_0 is the threshold voltage, r is the slope resistance, I_{av} is the average current, and $I_{\rm rms}$ is the RMS current. For the calculations of thyristor and diode, the corresponding threshold voltage and slope resistance are obtained from datasheet. The turn-on losses of thyristor and diode are neglected. Then by substituting the data into (38), the on-state power loss for each individual component is obtained. That is further scaled to get the loss for each module, and then finally the total extra power loss for the 12-pulse inverter, which is calculated to be 2.954 MW. Consider the 1500 MW rating of the HVDC system and that the TBCCs are only installed at inverter side, the percentage of loss increase per converter station is calculated as $2.954/1500/2 = 0.0985\%$. It will increase the capitalized cost of converter station. However the economic savings of CF elimination are significant and can potentially justify the increased cost. Firstly the proposed method improves the availability of the UHVDC system, as the system may not need to be blocked and is able to ride through the inverter AC faults. The resulting additional electrical energy that can be transmitted with the proposed method is significant and directly results in cost savings. Secondly due to the ability of transmitting active power during faults, the economic savings can be achieved from 1) the reduction of the level of load shedding and activation of spinning reserve at inverter side and 2) the reduction of the level of generation tripping at rectifier side. Consider the high power rating of UHVDC and the restoration time of the tripped generators (up to hours), the potential savings are significant. Thirdly, the risks of system instability and blackout due to CF are reduced with the proposed method. As the number and rating of UHVDC systems continue to increase, the risks of AC system instability and blackout are increased. Consider the potentially huge economic loss from these risks, the savings can be significant.

VII. Discussion and Comparison

In this section, a comprehensive comparison is made between the proposed method and the method from [23]. The aspects of 1) system performance; 2) component usage & cost; 3) efficiency and 4) control complexity are considered.

In terms of system performance, the proposed method is able to achieve the elimination of CF while the method in [23] is to mitigate CF. It is due to the difference of controllability between TBCC module and the APT-DFBM. The TBCC module has full controllability of its capacitor voltage during operation, and hence can control the additional commutation voltage being provided. The commutation voltage provided by APT-DFBM cannot be actively controlled and is mainly determined by the DC current and the pre-determined size of the capacitor. Therefore it is difficult for APT-DFBM to provide a larger voltage-time area for successful commutations during serious faults with a very large AC voltage drops.

To facilitate the comparison of component usage & cost, the same single-phase fault as described in [23] has been simulated using the proposed method. The required voltage level from TBCC to achieve CF elimination is 33 kV and the operating voltages of $C1a$ and $C2a$ are 40 kV. According to the analysis in Section V, the maximum voltages experienced by $T1/T2, T3a/T4a$ and $T5a/T6a$ are 33 kV, 73 kV and 40 kV, respectively. Consider the same acceptable steady-state voltage of 4 kV for each thyristor, the numbers of thyristors for $T1/T2, T3a/T4a$ and $T5a/T6a$ are 9, 19 and 10, respectively. Therefore the total number of thyristors in the TBCC module is $9 \times 2 + 19 \times 2 + 10 \times 2 = 76$. Further considering the capacitors and inductors from commutation circuit, the number of component used and the associated cost for the TBCC module is higher than that of the APT-DFBM module ($8 \times 10 = 80$ thyristors). It is understandable as better controllability is achieved with TBCC at the cost of additional components. To achieve complete elimination of CF under 100% voltage drop as proposed in this paper, more TBCC modules are required and results in higher investment cost. However, the practical implementation of the proposed method will always be a tradeoff between the investment cost and the potential economic savings. For example it may not always be necessary to design the TBCC for 100% voltage drop, given that CFs are mostly caused by remote faults with limited AC voltage drops.

For comparison of efficiency, the same TBCC module with 33 kV is used. Using the calculation method from Section VI but for the 500 kV/2kA system, the loss is calculated to be 0.432 MW. This is 0.0432% increase of power loss, which is lower than the 0.062% calculated in [23]. It is because only one thyristor element is in conduction during normal operation ($T1$ or $T2$) for the TBCC module, while there are two in the APT-DFBM.

In terms of control complexity, the required measurement signals for each TBCC module are the current through the module and the main capacitor voltage. For the APT-DFBM module, in addition to these two signals, additional signals for fault detection and fault clearance are required. Furthermore the TBCC only needs to control its main capacitor voltage during operation. The APT-DFBM module has several control modes during operation and coordination between them is required depending on the fault and capacitor voltage. Such coordination is not required for the TBCC modules.

VIII. Conclusion

The TBCC module has been proposed in this paper to achieve the elimination of CF for UHVDC systems. The module is based on thyristors only hence the proposed method is suitable for UHVDC systems with higher power/current ratings. Detailed operating principles, capacitor voltage control strategy and mathematical analysis of the TBCC module have been explained, and the selection of parameters has been given. To validate the effectiveness of the proposed method, comparisons are made with CCC-HVDC and LCC-HVDC using systems rated at 500 k V/3 kA. Additional simulation results of the HVDC with larger AC systems (IEEE 39-bus system) at both rectifier and inverter sides have been presented. 800 kV/4 kA system is

further developed and simulated to demonstrate the capability of the proposed method in application to UHVDC systems. In addition, the analysis of voltage & current stresses of thyristors and the estimation of power losses have been carried out. Comparisons of the proposed method with that in [23] have been made.

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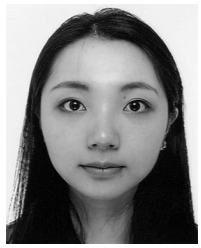

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