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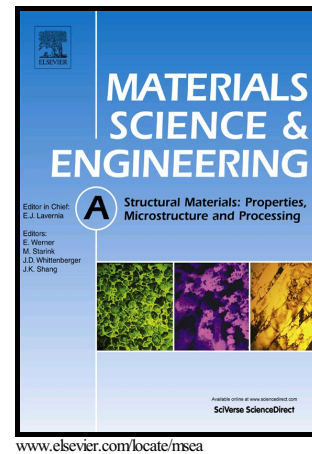
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High temperature nanoscratching of single crystal silicon under reduced oxygen condition

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Abstract

In-situ high temperature nanoscratching of Si(110) wafer under reduced oxygen condition was carried out for the first time using a Berkovich tip with a ramp load at low and high scratching speeds. Ex-situ Raman spectroscopy and AFM analysis were performed to characterize high pressure phase transformation, nanoscratch topography and nanoscratch hardness. No remnants of high pressure silicon phases were observed along all the nanoscratch residual tracks in high temperature nanoscratching, whereas in room temperature nanoscratching, phase transformation showed a significant dependence on the applied load and scratching speed i.e. the deformed volume inside the nanoscratch made at room temperature was comprised of Si-I, Si-XII and Si-III above different threshold loads at low and high scratching speeds. Further analysis through AFM measurements demonstrated that the scratch hardness and residual scratch morphologies i.e. scratch depth, scratch width and total pile-up heights are greatly affected by the wafer temperature and scratching speed.

Keywords: High temperature; Nanoscratching; Single crystal silicon; Polymorphs

1. Introduction

Silicon is a technologically crucial material and is the workhorse of the semiconductor industry due to its excellent stability, wear resistance and abundance. However, bulk wafers of single crystal silicon exhibit poor machinability at room temperature owing to their relatively low fracture toughness and high nanoindentation hardness. It is a common belief that the yield strength and hardness of silicon would reduce at high temperature. As such, the fracture toughness of silicon improves and its hardness decreases which would ease the plastic deformation and improve the machinability [1, 2].

Molecular dynamics (MD) simulation studies have been conducted on high temperature nanometric cutting of silicon for the sake of making important contributions to our fundamental understanding of the occurring processes at the atomic scale at elevated temperatures [1, 3-5]. It has been revealed that MD simulation is a robust numerical analysis tool in addressing a range of complex nanometric cutting problems that are otherwise difficult or impossible to understand using other methods. For example, the mechanics of high temperature nanometric cutting of silicon is influenced by a number of variables such as machine tool performance, cutting conditions, material properties, and cutting tool performance (material microstructure and physical geometry of the contact) and all these variables cannot be monitored online through experimental examination. However, these could

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suitably be studied using an advanced simulation based approach such as MD simulation. Although MD simulation offers a unique opportunity to explore the atomic level discrete processes of nanometric cutting/scratching of silicon under desired conditions, there exists some other phenomena which are impossible to be investigated using MD simulation, attributable to either the lack of a proper interatomic potential function or the excessive intricacy of the phenomenon. For instance, the available potential functions are not robust in describing and capturing all the structural phases of silicon; hence phase transformation mechanisms during nanometric cutting/scratching at room and elevated temperatures cannot be understood through MD simulation. Furthermore, the MD simulated depth of cut is only several nanometres, which is much smaller than the actual depth of cut (~ several hundred nanometres to tens of micrometres). Consequently, high pressure phase transformation cannot be simulated under such condition. Therefore, experimental determination of the formation of polymorphs is required. It should be noted here that the material removal mechanism in scratching is similar to that in cutting/machining. Hence, it is possible to substitute the complicated cutting/machining with a relatively simple scratching so as to study material removal mechanism involved in cutting/machining [6].

In this paper, the focus will be on the experimental studies of the pressure-induced silicon polymorphs, nanoscratch topography and nanoscratch hardness in nanoscratching of silicon at room and elevated temperatures. To this end, using the state-of-the-art nanoindentation equipment, in-situ high temperature nanoscratching trials on single crystal silicon wafer under inert gas are performed and ex-situ characterization techniques, such as Raman spectroscopy and atomic force

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microscopy (AFM) are employed to shed some light on the aforementioned processes.

2. Literature review

The previous work on nanoscale cutting/scratching/indentation by MD simulation has primarily focused on demystifying the material removal mechanisms at “room temperature”. What is known from these studies is that the current pool of knowledge on the nanometric cutting/scratching/indentation at elevated temperatures is still sparse. Only limited work has been done so far on studying hot nanoscale cutting/scratching/indentation by MD. In preliminary investigations performed by the authors, hot nanometric cutting of single crystal silicon and silicon carbide on different crystal orientations was compared with the cutting at room temperature (27°C) so as to characterize the cutting mechanics such as material flow, stagnation region, specific cutting energy, cleavage and defect-mediated plasticity [1, 3-5, 7-9]. Fang *et al.* [10] and Liu *et al.* [11] performed MD simulations to examine the variation in Young’s modulus, hardness and elastic recovery of copper, diamond and gold during nanoindentation at high temperatures (up to 327°C). They concluded that Young’s modulus, hardness and the extent of elastic recovery decreases with the increase of temperature. Hsieh *et al.* [12] used MD simulation to investigate the effect of temperature on maximal normal forces and elastic recovery during nanoindentation of copper. They reported a reduction in the aforementioned parameters with an increase in the substrate temperature.

On the experimental side, there is no study hitherto on high temperature nanometric cutting/scratching. However, there is a history of using ‘hot hardness’

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microindentation tests, beginning with Atkins and Tabor [13]. Nevertheless, instrumented hardness tests at high temperatures have a shorter history. Wheeler and co-workers [14-16] have described the general nano-mechanical test platform capable of performing variable temperature and variable strain rate testing. The thermal management and measurement techniques and vacuum nanoindentation have been discussed in their review papers. Similarly, Schuh and his colleagues [17, 18] produced an elegant discussion of the technical issues surrounding high temperature nanoindentation in ambient and inert environments.

In 1996, Suzuki and Ohmura [19] performed ultra-microindentations on {110} surfaces of single crystal silicon in the temperature range of 20-600°C and concluded that below 500°C, the temperature-insensitive hardness is determined by the transformation to the metallic β -tin phase, which amorphizes or nanocrystallizes during unloading, while above 500°C, plastic deformation due to dislocation activity causes temperature-dependent hardness. Smith and Zheng [20] modified a depth sensing indentation instrument to measure small scale hardness and elastic modulus of glass, gold, and single crystal silicon at 200°C. The hardness and elastic modulus of soda lime glass and gold were found to be lower than that at room temperature. In contrast, indentation testing of Si(100) at 200°C produced a similar hardness value to that obtained at room temperature, although the modulus was reduced, from 140.3 to 66 GPa. In addition, the well-known 'pop out' event, which is observed during unloading of a silicon indentation at room temperature, disappeared at 200°C. Beake and Smith [21] demonstrated that mechanical properties of fused silica exhibit a completely different temperature dependence from those of soda-lime glass during high temperature nanoindentation at 400°C, since fused silica is an anomalous glass.

Xia *et al.* [22] observed that the surface hardness of Fe-40Al, an iron aluminide, is higher and the elastic modulus is lower at elevated temperatures (400°C) than the corresponding values at room temperature. Lund *et al.* [23] investigated the effect of temperature during nanoindentation of pure platinum. They reported that the transition from elastic to plastic deformation takes place at progressively lower stress levels as temperature is increased. By adapting a commercial nanoindenter to allow testing at up to 200°C, Schuh *et al.* [24] explored the deformation map of two type of metallic glasses, and found that increasing the temperature at a constant indentation rate sees the gradual emergence of homogeneous flow, as thermal relaxations allow dissipation of strain localization into general viscous flow. Nanoindentation studies of single crystal Ni-base superalloy CMSX-4 oriented in the $\langle 001 \rangle$ and $\langle 110 \rangle$ directions were conducted by Sawant and Tin [25] over a range of temperatures from 30°C to 400°C. Trelewicz and Schuh [26] carried out high-temperature nanoindentation experiments to assess the activation enthalpy for deformation of nanocrystalline Ni-W alloys, for grain sizes between 3 and 80 nm. They reported that thermal softening becomes less pronounced at finer grain sizes, and the activation enthalpy has an apparent inflection at a grain size near $\sim 10\text{-}20$ nm, in the vicinity of the Hall-Petch breakdown. It should be noted here that large amount of studies have been performed on the high temperature nanoindentation of various materials [27-36]. However, for the sake of brevity, only studies on silicon are discussed in the following paragraphs. Bradby and his co-workers [37, 38] reported that in hot nanoindentation of silicon, increasing temperature enhances the nucleation of Si-III and Si-XII during unloading but the final composition of the phase transformed zone is also dependent on the thermal stability of the phases in their respective matrices.

Besides, they found that the region under the indenter undergoes rapid volume expansion at temperatures above 125°C during unloading. Moreover, polycrystalline Si-I was the predominant end phase for indentation in crystalline silicon whereas high-pressure Si-III/Si-XII phases were the result of indentation in amorphous silicon. They also concluded that the Si-II phase is unstable in a c-Si matrix at elevated temperatures. In a similar work, Domnich *et al.* [39] carried out high-temperature nanoindentation using Berkovich probe and observed that up to a certain critical temperature (350°C), the nanoindentation hardness of silicon is dictated by the pressure required to transform the semiconducting Si-I phase into the metallic Si-II phase of silicon. However, no phase transformation was observed above 350°C and it was suggested that the nanoindentation hardness in silicon above 350°C is dictated by dislocation glide. From what was discussed above, it can be inferred that although some studies have been performed so as to improve our understanding of high temperature nanoindentation behaviour, no methodical work is available to date on the area of high temperature nanometric cutting/scratching of silicon. It might be argued that both techniques are beneficial in understanding and characterizing the materials; nevertheless, nanometric cutting/scratching unlike nanoindentation is dominated by deviatoric stresses carrying pronounced component of shear. Consequently, the stress distribution in nanometric cutting/scratching is considerably different from that of nanoindentation; hence the results are not transferable. Accordingly, it is suggested that there is a strong need to understand the high temperature nanometric cutting/scratching mechanisms of hard-brittle materials such as silicon.

3.1. Equipment

Nanoscratching trials were performed on a MicroMaterials Ltd. (MML) nanoindenter called NanoTest Vantage. This equipment permits testing at elevated temperatures with low thermal drifts under reduced oxygen/purged condition and controlled humidity levels, which offers the perfect capability for testing materials in extreme conditions. Figure 1 demonstrates the heating arrangement in the MML NanoTest Vantage system.

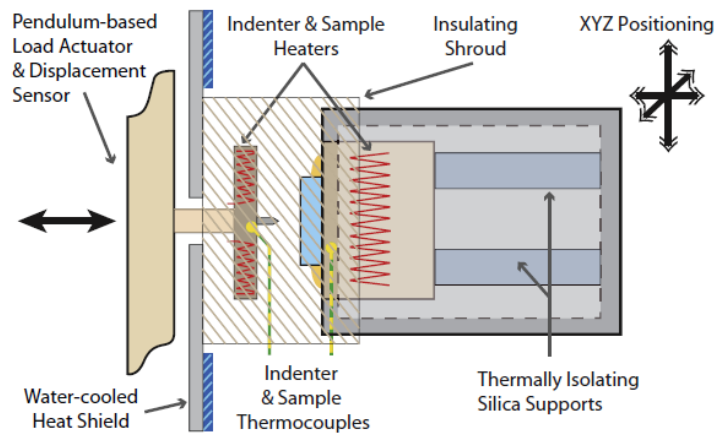


Figure 1: Schematics of the heating arrangement of NanoTest Vantage [14]

It is known that silicon is reactive with oxygen at high temperatures; hence performing nanoscratching trials under reduced oxygen condition is indispensable. NanoTest Vantage system uniquely features a chamber which can be over-pressurized with a shield gas i.e. high purity Argon to surround the hot zone during testing. Figure 2 shows the configuration of NanoTest Vantage system employed for conducting the nanoscratching tests.

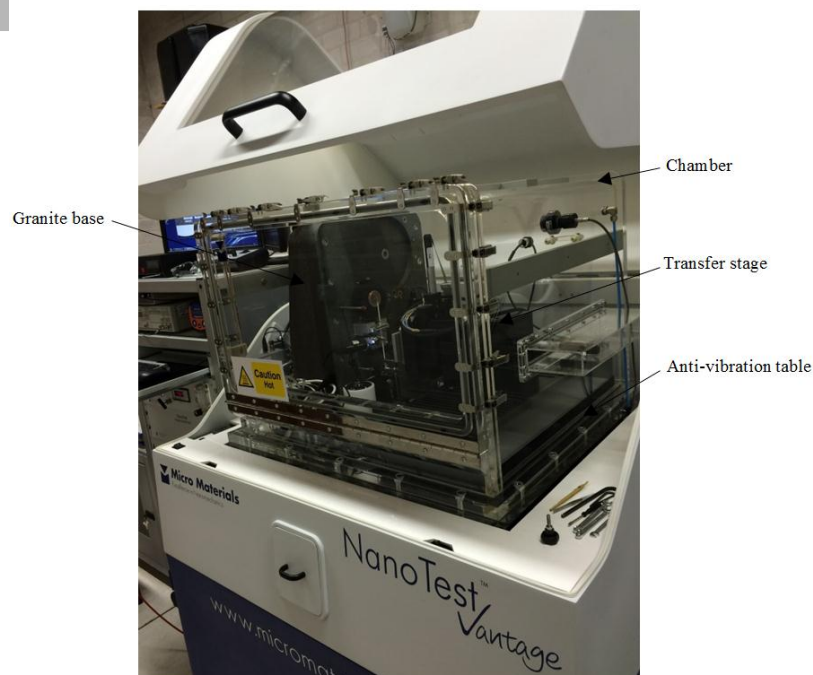


Figure 2: NanoTest Vantage equipment used to perform nanoscratching trials

3.2. Wafers and nanoindenters

The polished undoped n-type single crystal silicon wafers with the orientation (110) of size $10\times 10\times 0.5$ mm were utilized for the experiments. As pointed out recently by Gerbig *et al.* [40], the augmented deviatoric stress, especially the shear stress, for the Si(110) surface as compared with the Si(100) and Si(111) surfaces could ease the plastic deformation processes leading to decreased transformation pressures in silicon. Moreover, there is little work on the material removal mechanisms of the Si(110) surface in nanoscratch testing [41].

Prior to trials, the silicon wafers were first ultrasonically cleaned for 20 min in acetone, then dipped into 2% HF (Hydrofluoric) aqueous solution for 60 min to remove the oxide layers, followed by a thorough rinse in de-ionized water. The surface roughness of the etched wafers was measured in four areas using a white light interferometer (Zygo CP300). The etched wafers had an average flatness of

~239±65 nm in terms of PV height while average Ra was measured as ~0.56±0.06 nm.

Berkovich nanoindenter with a nominal tip radius of ≥ 50 nm and having 3-sided pyramidal faces forming an angle of 65.03° with the vertical axis was employed in the nanoscratching experiments reported here. The Berkovich nanoindenter would provide the more pragmatic conditions which could be confronted in actual applications. In addition, the use of this type of nanoindenter would lead to the much higher local pressure with similar load thus would be beneficial in elucidating the pressure-induced phase transformation problems.

3.3. Experimental procedure

Nanoscratching experiments were carried out at substrate temperatures of 25°C and 500°C using a linearly increasing load spanning from 0 to 10 mN along a total scratch length of $100\ \mu\text{m}$ at two constant speeds of $0.1\ \mu\text{m/s}$ (low speed) and $10\ \mu\text{m/s}$ (high speed). At each scratching speed, three scratches were produced. The nanoscratches were made along the Si<100> direction. Nanoscratching trials at room temperature (25°C) were conducted under atmospheric conditions whereas hot nanoscratching experiments were performed under reduced oxygen condition through an overpressure of pure Argon in the chamber. The amount of oxygen in the chamber was kept in the range of ~0.2-0.3% during the experiments. The experimental parameters and conditions used for the trials are summarized in Table 1.

Table 1: Nanoscratching conditions

Silicon wafer	Scratching direction	Temperature (°C)	Scratching speed ($\mu\text{m}/\text{s}$)	Ramp load (mN)	Total scratch length (μm)	Inert gas for high temperature testing
Si (110)	Si <100>	25 and 500	0.1 and 10	0-10	100	Argon

For the room temperature experiments, the wafer was glued with Cyanoacrylate onto a stainless steel disc and then fixed on the metal holder of the nanoindenter machine. For the high temperature nanoscratch testing, the wafer was glued onto the hot stage using high temperature cement, as shown in Figure 3.

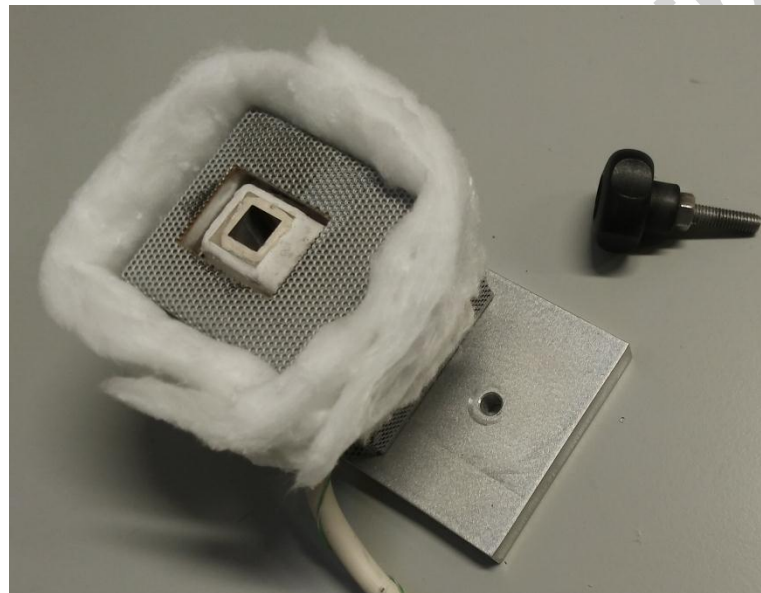


Figure 3: Glued silicon wafer on the hot stage

To perform high temperature nanoscratching experiments, the wafer was heated at a low rate of $1.6^{\circ}\text{C}/\text{min}$ to reach the target temperature. It should be mentioned that the nanoindenter was not independently heated. The swift heat transfer and thermal gradients between the heated wafer and the cold nanoindenter tip could lead to a

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substantial thermal drift, which influences the reliability of the results. In order to minimize the thermal drift, the wafer-tip contact was achieved and wafer-tip was kept in contact during the heating process. Note that after performing high temperature nanoscratching, the wafer was cooled in the chamber at the same rate ($1.6^{\circ}\text{C}/\text{min}$) until the room temperature was reached. Figure 4 illustrates a close snapshot of experimental system during high temperature nanoscratching. The nanoindenter and glued wafer on the hot stage were surrounded by mineral wool in order to reduce heat loss by convection and to stabilize the temperature.

After nanoscratching trials at room and high temperatures, a Thermo Scientific DXR Raman Microscope with a 532 nm diode-pumped solid state laser was used to detect the presence of crystalline and high pressure phases inside the scratches. Also, a Veeco Dimension 3100 atomic force microscope (AFM) with silicon tip was utilized to determine the topography of the nanoscratches.

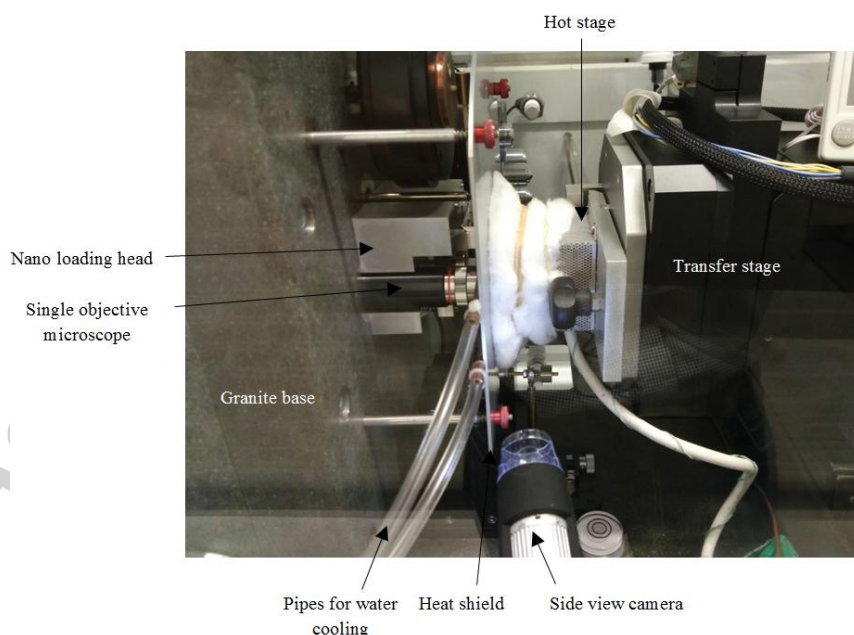


Figure 4: A close snapshot of experimental system during high temperature nanoscratching

4.1. Scratch topography

Figure 5 shows the typical topography of the residual nanoscratch measured by using the tapping mode AFM at four different positions. The cross profile topography shows a permanent pile-up (vertical height from a-b and a-d illustrated in Figure 5) at the both edges of track, which is closely associated to the plastic extrusion of silicon during nanoscratching. The heights of pile-ups are found to be asymmetric, plausibly due to the indenter tilt [42].

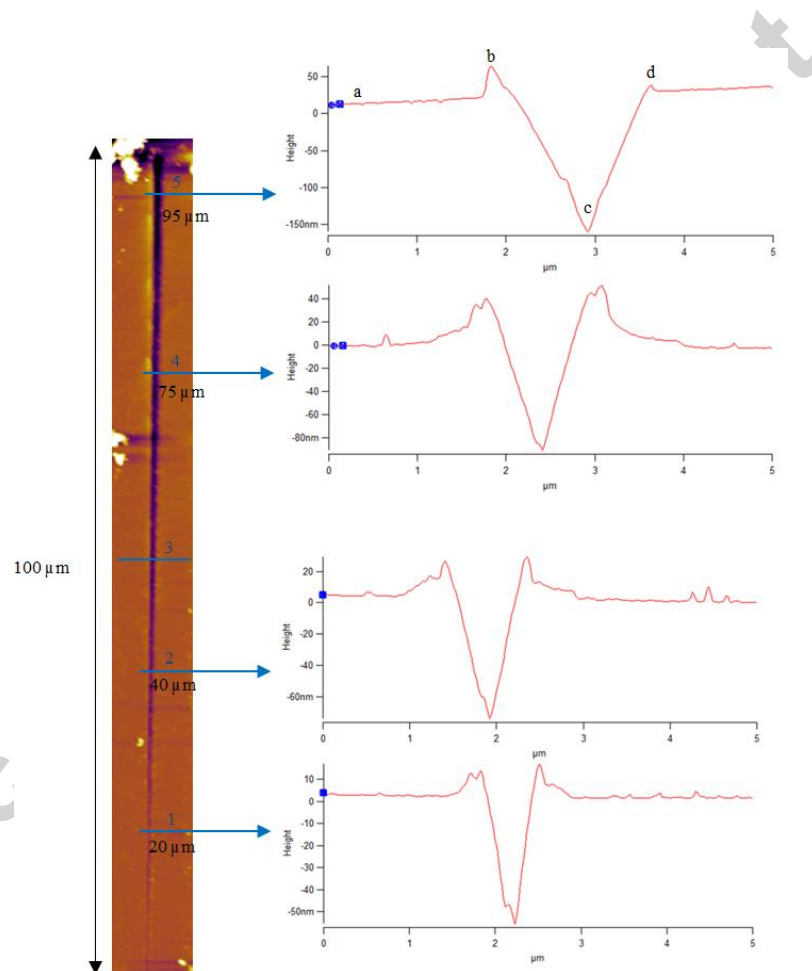


Figure 5: Typical AFM image of the nanoscratch and cross section profiles measured at four different positions. Scratch depth (vertical height from a-c), scratch width

(horizontal width b-d) and pile-ups (vertical height from a-b and a-d) are shown on the top profile.

Figure 6 illustrates the variation of scratch depth, scratch width and total pile-up heights at four various positions of the nanoscratch shown in Figure 5 during nanoscratching at room and high temperatures and at two scratching speeds i.e. low speed (0.1 $\mu\text{m/s}$) and high speed (10 $\mu\text{m/s}$). It can be seen that with the increase of applied load and consequently pushing more material to the side of the scratches, the residual scratch depth, scratch width and total pile-up heights increase along the scratch length. Furthermore, the aforementioned parameters increase with the rise of temperature as a result of thermal softening. It is also found that the residual scratch morphologies are strongly affected by the scratching speed i.e. scratch depth, scratch width and total pile-up heights decrease with the increase of scratching speed. It can be inferred that the degree of nanoscale elastic recovery during nanoscratching is more serious at high speeds than at low speeds. The obtained results are in accord with the trend reported by Li *et al.* [43], where the residual scratch depth of K9 glass decreased with the increase of the scratching speed at the same normal load.

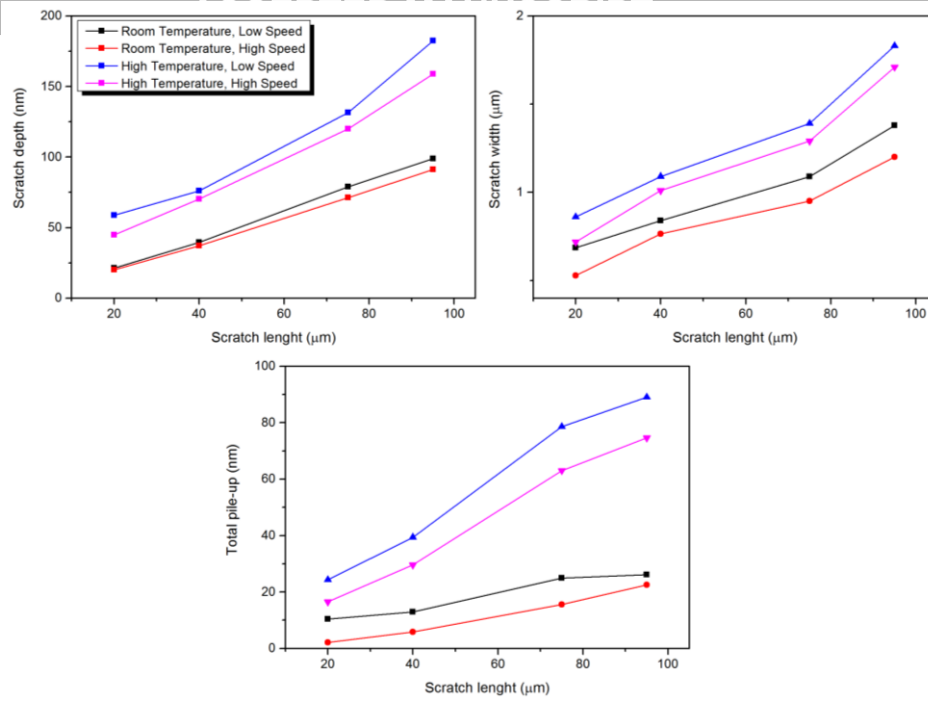


Figure 6: Variation of scratch depth, scratch width and total pile-up heights along the scratch length with the temperature and scratching speed

Nanoscratch hardness (H) can be employed so as to ascertain the resistance of material to the scratch, and it is described as the response of material under dynamic deformation of the surface. This parameter is defined as the ratio of the vertical load (P) to the surface area of the tip-sample contact or the contact area projection onto the horizontal plane which depends on the residual scratch width (b):

$$H = k \frac{P}{b^2} \quad (1)$$

where k is the nanoindenter tip shape factor, which is dependent on the tip configuration. For a Berkovich indenter, this factor is 2.31 [44]. The average values of scratch hardness obtained from the trials are listed in Table 2. Due to an effective reduction in the shear stress at high temperatures, the scratch hardness has lower magnitudes at high temperatures. Moreover, the scratch hardness increases as the scratching speed increases, signifying a strain rate strengthening of the silicon

material at higher scratching speed. In scratch hardness, the effective strain rate can be defined as the ratio of the scratching speed to the scratch width. The strain rate hardening effect means that the material provides a greater resistance to plastic deformation [45].

Table 2: Scratch hardness at different conditions

Nanoscratching condition	Scratch hardness (GPa)
Room temperature, Low speed	12.2
Room temperature, High speed	16.7
High temperature, Low speed	7.4
High temperature, High speed	9

4.2. Nanoscratching-induced phase transformation

In order to identify the existence of high pressure phases of silicon inside the nanoscratch tracks, Raman spectroscopy was employed. For each scratch, the Raman spectra were collected at five different locations i.e. at the position of blue lines shown in Figure 5. It should be mentioned here that the reported phases in this study are the stable or remnant phases since the residual nanoscratch impressions were measured at room temperature after the nanoscratching experiments. Figure 7 and Figure 8 illustrate the Raman spectra of silicon obtained from the five various locations of the scratch made at room and high temperatures, respectively, at low (0.1 $\mu\text{m/s}$) and high (10 $\mu\text{m/s}$) scratching speeds. On all spectra, the single line at 519.4 cm^{-1} can be observed, which is close to the reported 520 cm^{-1} optical mode of bulk silicon (Si-I). Note that a small amount of stress may cause a shift. It can be

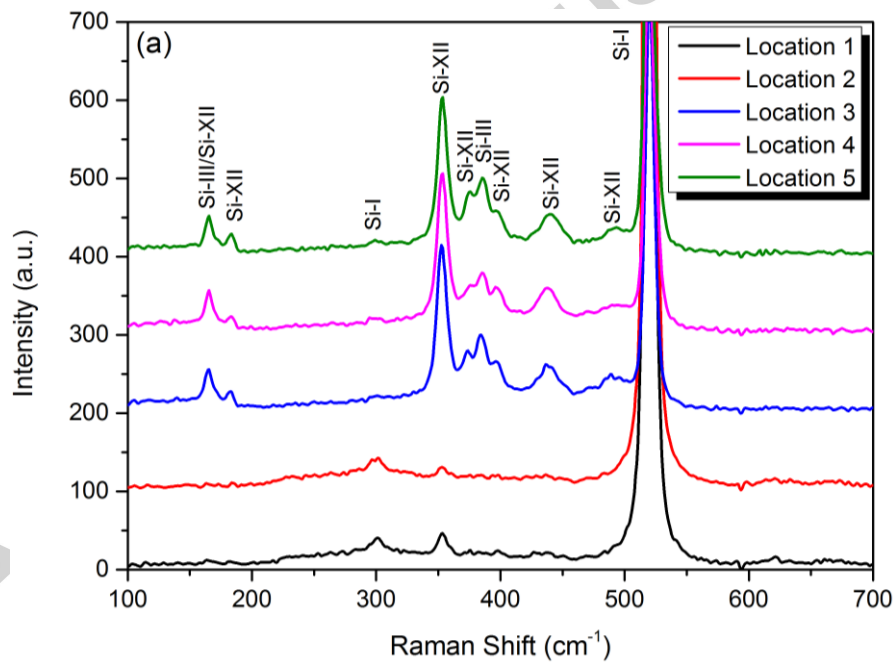
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inferred from Figure 7a that while room temperature nanoscratching at low scratching speed, the nanoscratch is composed of Si-I (bands at 520 and 300 cm^{-1}) and high pressure phase Si-XII (band at 352 cm^{-1}) when the scratching load is lower than ~ 4 mN, corresponding to the locations 1 and 2 in Figure 5. However, the intensity of the peak corresponding to Si-XII is very low, signifying that the content of Si-XII is relatively small. Above the transition load of ~ 5 mN, the nanoscratch is formed of Si-I, Si-XII characterized by bands at 166, 182, 352, 374, 396, 440, and 491 cm^{-1} , and Si-III (bc8, body-centred cubic structure) identified by bands at 166 and 385 cm^{-1} . Both Si-III and Si-XII (r8, the rhombohedral distortion of bc8) are known to show semi-metallic electronic behaviours. It is of note that the band at 385 cm^{-1} predicted by Plitz *et al.* [46] for the bc8 structure, was attributed by Ge *et al.* [47] to Si-III together with other bands at 415 and 465 cm^{-1} . Nevertheless, the absence of these last bands would indicate that Si-III is in minor quantity in the nanoscratch track. This observation is in good agreement with the decompression path proposed by Gassilloud *et al.* [48]. It is informative to note that there are strong indications that the presence of metastable crystalline phases (Si-XII and Si-III) in the residual imprints can be a consequence of formation of β -tin silicon (Si-II) during contact loading of silicon [49]. In other words, metallic Si-II is formed during nanoscratching owing to the highly localized stresses underneath the indenter and subsequently is transformed to Si-III and Si-XII, accompanied by $>10\%$ volume increase [6], which contributes to the elastic recovery of the scratched surface.

Interestingly, above the transition load of ~ 5 mN, the probability of forming Si-III and Si-XII phases was found to increase. However, the intensities remain almost

constant for these phases, suggesting that the volume of Si-III and Si-XII phases does not change at scratch loads higher than ~5 mN.

The literature suggests that the mode of unloading/release of the pressure plays a crucial role in reverse transformation from metallic phase to crystalline phases i.e. upon slow unloading, a crystalline phase of Si-XII and Si-III may persist whereas Si-IX, amorphous silicon and Si-I could be obtained upon fast unloading. The Raman spectra shown in Figure 7b demonstrate that the nanoscratch made at high scratching speed is composed of Si-I when the scratch load is below ~7.5 mN. At higher loads i.e. ~9.5 mN, some small remnants of Si-XII and Si-III can be observed inside the scratch. As mentioned above, the high scratching speed corresponds to a high unloading rate, which likely leads to the formation of the Si-I.



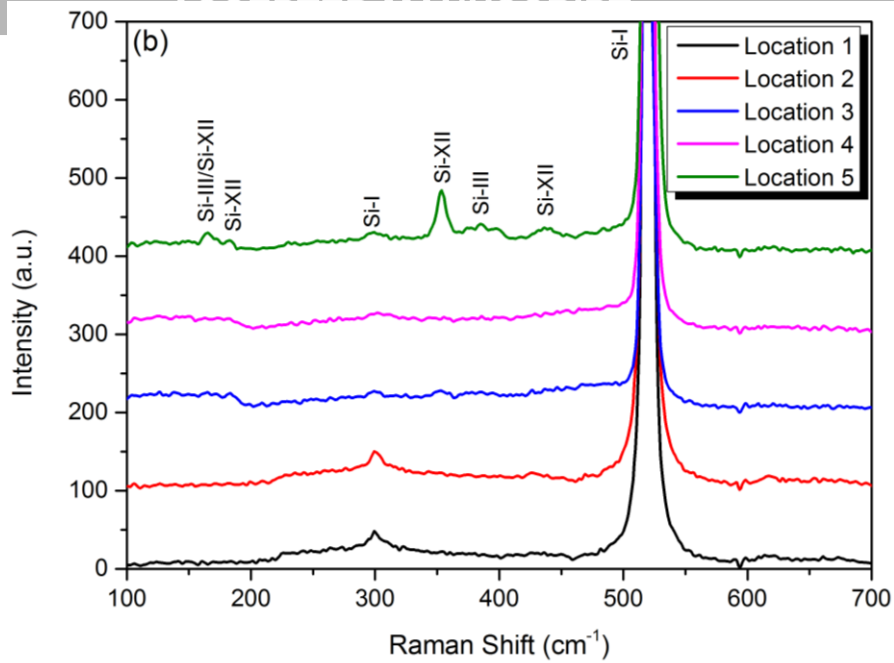


Figure 7: Raman spectra collected from five different locations of the nanoscratch shown in Figure 5, and fabricated under room temperature condition at constant scratching speed of: a) 0.1 $\mu\text{m/s}$ (low speed) and b) 10 $\mu\text{m/s}$ (high speed)

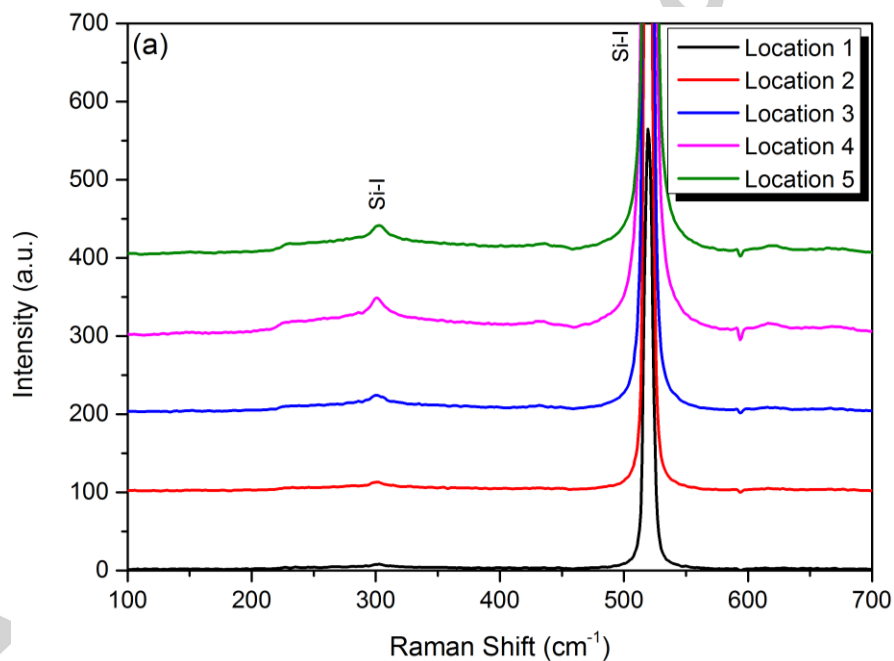
As evident in Figure 8a and Figure 8b, the Raman peaks for the Si-III and Si-XII phases disappear and no remnants of polymorph phases are detected all along the nanoscratch residual track when high temperature nanoscratching is performed at low and high speeds. This means the Si-III/XII \rightarrow Si-I phase transition occurs during the nanoscratching at high temperature of 500°C. This observation agrees with the idea that high temperature promotes the transition of metastable silicon phases (Si-III and Si-XII) into thermodynamic stable Si-I [39]. In nanoindentation process of silicon, Domnich *et al.* [39] observed that when the temperature was above 300-350°C, only cubic diamond silicon was detected, which is in excellent agreement with the obtained results of high temperature nanoscratching in our study. Moreover, there is some evidence that Si-III and Si-XII transform back to Si-I with annealing. Ruffle *et al.* [50] reported that the intensity of the peaks related to the Si-III and Si-

XII phases drops with increasing annealing time at 175°C, and after 120 min, none of these phases are detected and the Raman spectrum is similar to that of pristine silicon. Moreover, they claimed that the lifetime of the Si-III/XII is temperature dependent, and it is over 1 min at 320°C and at ambient pressure. Taking into account the high temperature nanoscratching at 500°C performed in this study, it can be assumed that annealing at 500°C with the cooling rate of 1.6 °C/min can commence a fast Si-III/XII → Si-I phase transition during the trials. Hence, the only stable phase which is detectable from the Raman spectra shown in Figure 8 is the pristine silicon (Si-I). The obtained results in this study are also consistent with the high power laser irradiation of the indentations carried out by Zeng *et al.* [51], where rapid Si-III/XII → Si-I phase transition within 1s was realized.

It should be noted here that other metastable phases like hexagonal diamond (Si-IV), which is characterized by a broad band at 510 cm⁻¹, or amorphous silicon (a-Si), which is characterized by broad bands at near 170 and 490 cm⁻¹, were not observed within the residual scratches while nanoscratching of silicon at room temperature and high temperature of 500°C using the adopted ramp load ranging from 0 to 10 mN at two constant speeds of 0.1 μm/s (low speed) and 10 μm/s (high speed). A possible hypothesis is that the adequate pressure for amorphization of silicon is not attained inside the scratch tracks. It can be also postulated that a-Si crystallizes during high temperature nanoscratching trials since very small volumes of a-Si typically do not require annealing temperatures exceeding 550°C in order to exhibit significant crystallization [52]. Meanwhile, there is some evidence that nanoclusters of a-Si can crystallize at temperatures as low as 70°C [53, 54]. Therefore, it is not surprising to observe the absence of a-Si within the scratch tracks. However, there might exist a

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small amount of residual a-Si within the phase transformed zone, yet its amount (if present) should be very limited which cannot be detected since Raman spectroscopy itself is not very sensitive and trace amounts may not be detectable with this technique. This may be resolved by using more advanced Raman techniques such as surface-enhanced Raman scattering (SERS) and tip-enhanced Raman scattering (TERS) etc. It can be argued that cross-sectional transmission electron microscopy (XTEM) analysis can be employed to further investigate the presence of a-Si in the scratch. However, the focused ion beam (FIB) can damage the cross-sectional sample which in turn could generate a-Si within the scratch.



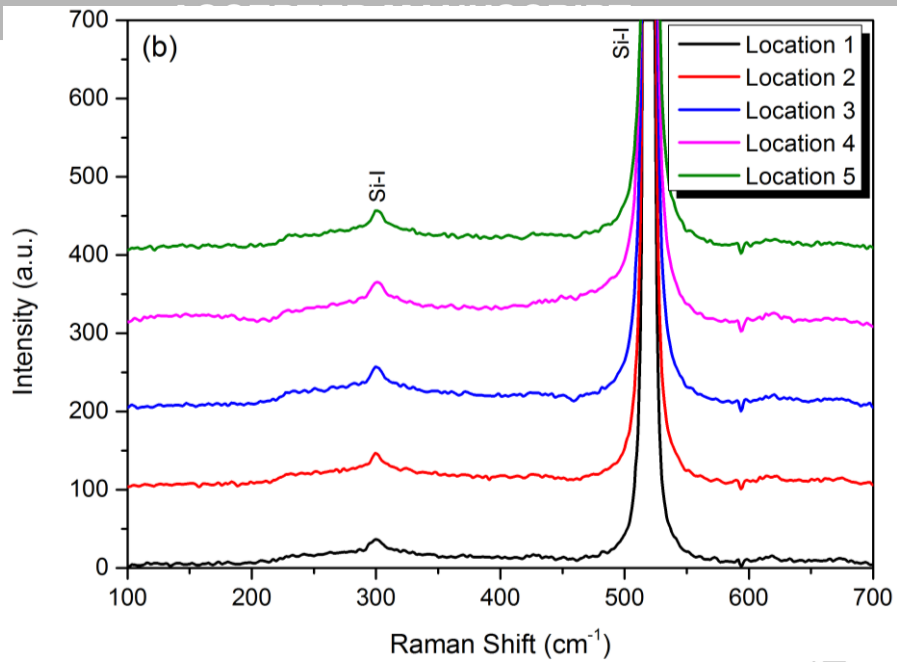


Figure 8: Raman spectra collected from five different locations of the nanoscratch shown in Figure 5, and fabricated under high temperature condition (500°C) at constant scratching speed of: a) 0.1 $\mu\text{m/s}$ (low speed) and b) 10 $\mu\text{m/s}$ (high speed)

4. Summary

Single crystal silicon nanoscratching experiments were performed at room and high temperatures to comprehend the influence of substrate temperature on the high pressure phase transformation, nanoscratch topography, nanoscratch hardness and condition of the tool tip in nanoscratching. The Raman spectroscopy results revealed that while room temperature nanoscratching at low scratching speed, above the transition load of ~ 5 mN, the nanoscratch is formed of Si-I, Si-XII and Si-III, and the probability of forming high pressure phases of Si-III and Si-XII increases above this load. Nevertheless, Si-III phase was found to be in minor quantity in the nanoscratch

track. At high scratching speed, small remnants of Si-XII and Si-III phases were detected when the scratch load was greater than a threshold value i. e. ~ 9.5 mN. When high temperature nanoscratching was carried out at low and high speeds, no remnants of polymorph phases were observed all along the nanoscratch residual track, suggesting the transition of metastable silicon phases (Si-III and Si-XII) into thermodynamic stable Si-I.

AFM measurements revealed that the residual scratch morphologies are profoundly influenced by the scratching speed viz. scratch depth, scratch width and total pile-up heights decrease with the increase of scratching speed. Moreover, the aforementioned parameters were observed to increase with the rise of temperature as a result of thermal softening. Further analysis through calculating the nanoscratch hardness showed a reduction at high temperatures. Additionally, the nanoscratch hardness was found to increase as the scratching speed increases, signifying a strain rate strengthening of silicon material at higher scratch speeds.

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Appendix

The wear mechanism of a diamond nanoindenter is very complex, involving chemical, physical, electrical, and mechanical interactions between diamond and substrate [55]. Figure A shows the scanning electron microscopy (SEM) micrograph of the nanoindenter tip taken by a Hitachi SU-6600 field emission scanning electron microscope (FE-SEM) after nanoscratching of silicon at room and high temperatures. As can be seen from the figure, under the present scratching conditions, the nanoindenter tip is not blunted i.e. mechanical wear does not occur for both cases owing to high surface hardness and wear resistance of diamond.

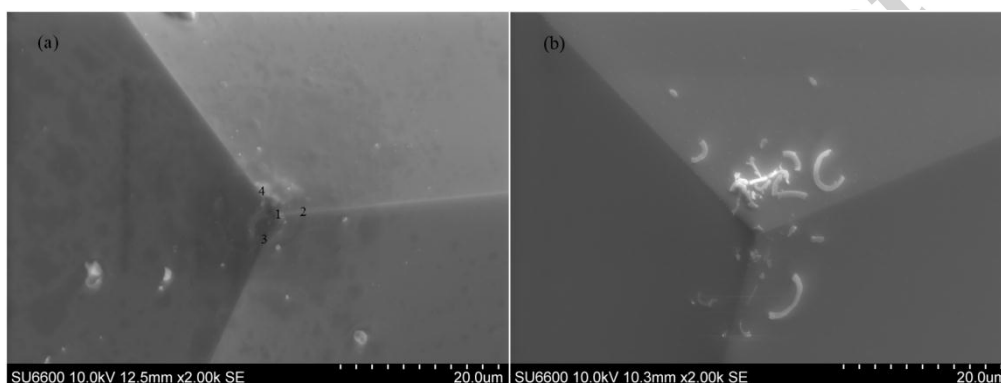
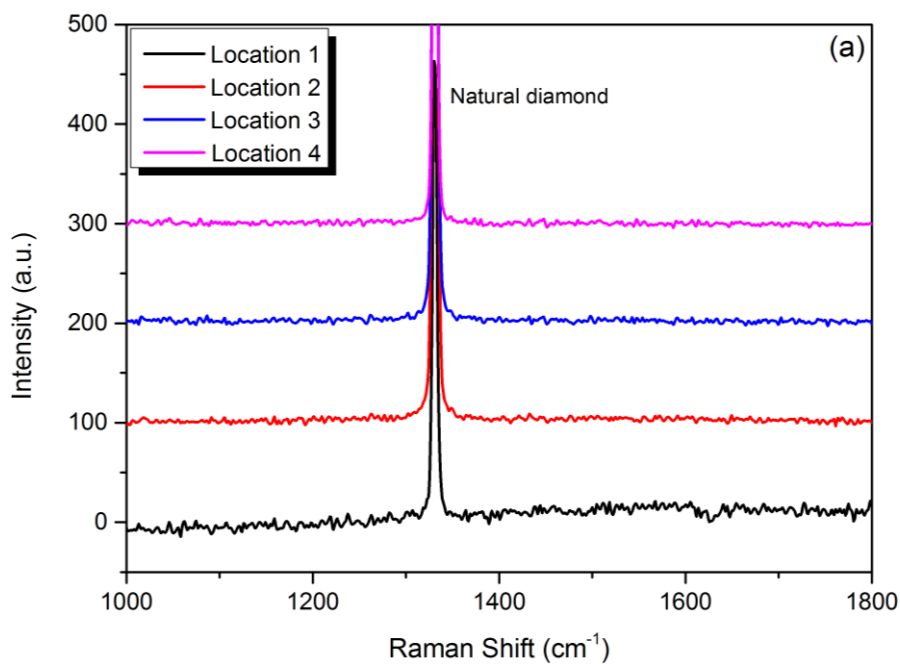


Figure A: SEM image of Berkovich nanoindenter tip used for nanoscratching at: a) room temperature and b) high temperature (500°C). The nanoindenter tips are not blunted under the present scratching conditions. The numbers "1, 2, 3, 4" in Figure Aa show the four locations used to collect Raman spectra.

In order to study the probable microstructural changes of the diamond nanoindenter tip, Raman spectroscopy was performed at four different points on the nanoindenter edges shown in Figure Aa. Figure B illustrates the Raman spectra of the diamond obtained from the four locations of the nanoindenter tip used for nanoscratching at room and high temperatures. The strong sharp peak at 1332 cm^{-1} corresponds to the first-order Raman peak of crystalline diamond [56]. Disordered graphite displays two

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distinct modes in the Raman spectrum: the G band centred at $\sim 1580\text{ cm}^{-1}$ and the D band centred at $\sim 1350\text{ cm}^{-1}$ [57]. However, such peaks were not observed in Figure B, suggesting that under the present nanoscratching conditions, no direct diamond to graphite transformation occurred. Hence, the diamond nanoindenter is not supposed to be worn by graphitization.



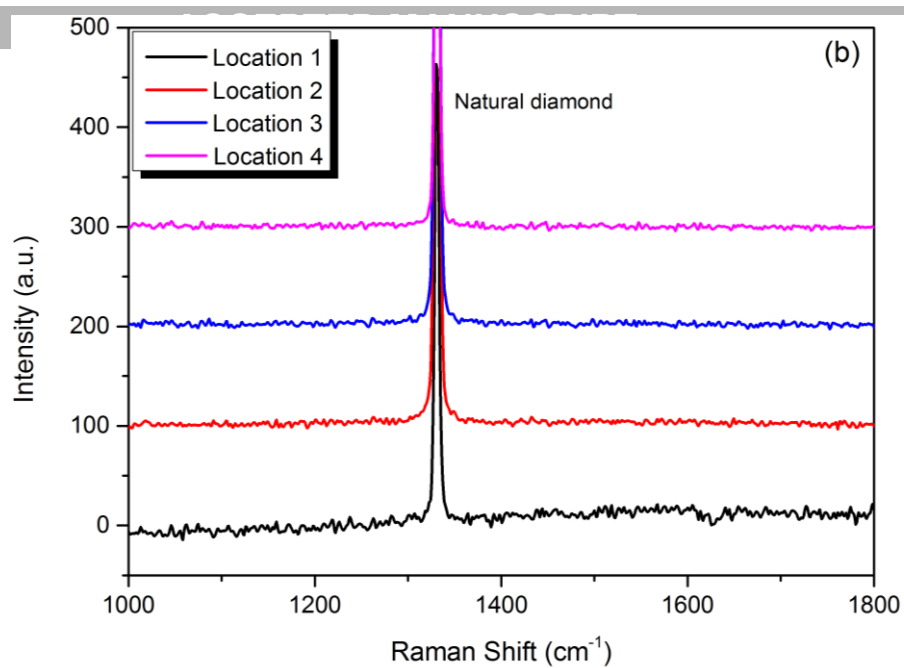


Figure B: Raman spectra collected from four different locations of the nanoindenter shown in Figure Aa, used for nanoscratching at a) room temperature and b) high temperature (500°C).

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