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Fullerene-based spin-on-carbon hardmask

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ABSTRACT

As feature sizes have diminished the need for extremely thin photoresist films has grown. Given the poor selectivity of typical resists with respect to silicon during plasma etching, it has become common to use an intermediate hardmask to transfer the pattern. Furthermore the use of trilayer etch stacks to amplify the achievable etch aspect ratio is becoming increasingly popular for critical layers. Here we introduce a new fullerene based spin-on-carbon layer for use in a multilayer etch stack. Carbon films of between 20 and 1270 nm were prepared by spin coating. Thin silicon films were deposited on the carbon layer and patterned using a thin photoresist. Patterns were transferred to the carbon layer with high anisotropy at resolutions down to 40 nm using an oxygen plasma, and then subsequently etched into the silicon substrate using an SF_6/C_4F_8 etch with high aspect ratio.

1. Introduction

The minimum feature size required by semiconductor devices has continued to shrink to enable increasing chip density, with '2× nm' flash and logic devices now available. As the resolution requirements have increased it has become necessary to adopt extremely thin photoresist films to mitigate problems such as mechanical collapse of resist features upon development [1]. We have previously demonstrated a high resolution, high sensitivity and high etch durability fullerene resist [2] capable of aspect ratios greater than 5:1 for 25 nm lines and spaces [3]. However, even with such a resist the overall etch depth is limited by the usable resist thickness. The use of a multilayer hardmask stack allows further increase of the achievable etching aspect ratio. Typically such a multilayer stack is formed by first coating the wafer with a thick amorphous carbon layer using chemical vapor deposition (CVD), and then overlaying this with a thin-silicon rich layer, which may either be spin coated or prepared by CVD [4,5]. Finally photoresist is spin coated on top of the silicon layer. A thin photoresist film is sufficient to pattern the thin silicon layer, avoiding pattern collapse issues, and the silicon is used as a hard mask to pattern the underlying carbon, giving a high aspect ratio carbon pattern suitable for subsequent etching of the silicon wafer. By alternating from silicon to carbon rich materials and vice versa the overall etch selectivity can be maximized. In order to improve manufacturability and decrease costs it would be beneficial to replace the use of chemical vapor deposition with spin-on hardmasks (both silicon and carbon) [6,7]. Previously a novolac:HSQ bilayer stack achieved 40 nm half-pitch resolution with an aspect ratio of 3.25:1 as well as isolated 40 nm lines with an aspect ratio of 20:1 [8]. However, distortion of the spin-on-carbon features during the final fluorine etch to silicon step, known as 'wiggling', is a significant concern for sub 40 nm patterning [9]. Glodde et al. have recently proposed that the absence of aliphatic hydrocarbons in the carbon layer can reduce 'wiggling' [10]. Here we present an initial study of several fullerene-based 'spin-on-carbons' (SoC) with very low levels of aliphatic hydrocarbons. In addition spin-on-hardmasks can suffer from low etching resistance [11], but the carbon-rich nature of the fullerene based SoC gives high etch durability.

2. Experimental

Silicon (100) substrates (Rockwood Electronic Materials, n-type) were used for all experimental procedures. Square chips, 2 by 2 cm in size, were cut from a wafer using a Disco DAD 321 wafer dicer. The samples were cleaned using semiconductor grade chemicals from Riedel-de Haën. Samples were washed ultrasonically for 15 min in isopropyl alcohol (IPA), then rinsed for 1 min in deionized (DI) water (Purite Neptune, 18.2 MΩcm). A hydrogen terminated surface was then prepared by dipping the substrates in H_2SO_4 (95–98%):H_2O_2 for 10 min, DI water for 1 min and dilute HF for 1 min, then rinsing in DI water for a further minute before drying with nitrogen. Substrates were stored under vacuum after preparation and used within 2 days.

We evaluated three spin-on carbon hardmasks from Irresistible Materials [12]. The spin-on carbon compositions were dissolved in a suitable solvent such as chloroform or anisole with a

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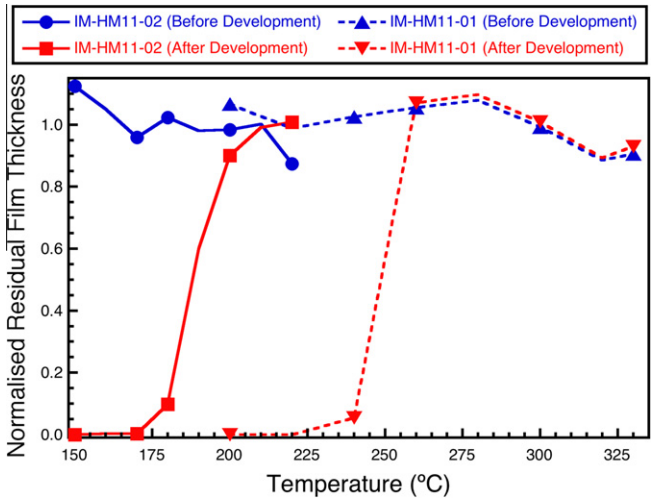

Fig. 1. The normalized film thickness of SoC films IM-HM11-01 and IM-HM11-02 before and after 'development' in an organic solvent (MCB:IPA 1:1). For temperatures above 190 °C IM-HM11-02 was not removed by the solvent rinse, whilst a temperature of 260 °C was required to render the IM-HM11-01 SoC insoluble.

concentration in the range 5–50 g/l. In this report, film thickness measurements were made for IM-HM11-01 and IM-HM11-02 films, whilst IM-HM11-03 was used for etching; further investigations to compare the performance of the different compositions across tasks are underway. Films of the SoC were prepared by spin coating on hydrogen-terminated silicon substrates with a speed varying between 800 and 2000 RPM for 60 s. After spin coating the film was baked for 2 min at temperatures of up to 330 °C. In order to enable further processing, the SoC should be rendered insoluble in typical solvents for resist and spin-on-hardmask to enable further processing. The elution behavior of films of IM-HM11-01 and IM-HM11-02 for thicknesses between 30 and 325 nm was tested as a function of the baking temperature. Fig. 1 shows the normalized film thickness of two formulations of the SoC (IM-HM11-01 and IM-HM11-02), before and after dipping in monochlorobenzene (MCB):IPA 1:1 solution. Prior to baking the thickness of IM-HM11-01 was ~320 nm, and the thickness of IM-HM11-02 was ~250 nm. For temperatures above 190 °C the IM-HM11-02 film was rendered insoluble, whilst a temperature of 260 °C was required to achieve the same for IM-HM11-01. Film thickness did not affect the elution results.

By varying the spin coating conditions and the concentration of the spin-on-carbon solution, films from 20 to 325 nm could be prepared in a single spin coating step. After coating films were stored in Entegris chip trays under ambient conditions in a cleanroom. No degradation of performance was seen even after more than a month of storage. The quality of the films was measure using a NanoWizard II atomic force microscope (JPK Instruments, UK) operating in intermittent contact mode at a tip velocity of 4 μm/s, employing pyramidal tipped Si cantilevers (PPP-NCL, Windsor Scientific, UK). Fig. 2(a) shows an AFM image of a typical bare Silicon substrate, and Fig. 2(b) and (c) shows SoC films baked at 225 and 375 °C respectively. It can be seen from the figure and from Table 1 that the SoC does not significantly degrade the smoothness of the silicon.

Table 1
AFM roughness measurements of two IM-HM11-01 films and a reference sample of silicon.

	IM-HM11-01 baked at 225 °C	IM-HM11-01 baked at 375 °C	Bare silicon
Average roughness (nm)	0.49	0.35	0.28
RMS roughness (nm)	0.60	0.45	0.35
Peak-to-valley roughness (nm)	7.24	4.50	4.57

As the carbon was rendered insoluble by heating it was possible to spin coat further carbon on top to increase the thickness. Fig. 3 shows an SEM (FEI XL30 SFEG) cross section of a carbon film of thickness 1.27 microns prepared by spinning five (IM-HM11-03) films of thickness ~250 nm on top of a each other with a heating step of 330 °C for 5 min between each spin coating.

After preparation of a ~300 nm IM-HM11-03 carbon film, a 40 nm thick silicon layer was deposited by sputtering at an argon pressure of 1×10^{-2} mbar for 2 min with 250 W RF power. Alternatively, Plasma Enhanced Chemical Vapour Deposition (PECVD) could be used to deposit the silicon film. Finally a photoresist was spin coated on top of the silicon layer. For this study either SAL601 (Shipley) or an in-house fullerene based resist were used. A post application bake of 90 °C for 10 min was applied to the SAL601; no post application bake was applied to the fullerene resist. The resist was patterned using an FEI XL30 SFEG scanning electron microscope equipped with a pattern generator (Raith Elphy Plus). SAL601 was exposed with an area dose 20 μC/cm^2 whilst the fullerene was exposed with a line dose of 10 nC/cm (~1.5 mC/cm^2). The SAL601 received a post exposure bake of 105 °C for 2 min and no post exposure bake was applied to the fullerene. Finally SAL601 was developed for 5 min in MF322 (Shipley) whilst the fullerene was developed in a 1:1 mixture of MCB:IPA. 80 nm halfpitch patterns and 40 nm sparse lines were patterned and then etched into the silicon thin film using an Oxford Instruments PlasmaPro NGP80 Inductively Coupled Plasma (ICP) etching system. Silicon substrates were attached using vacuum grease to a sacrificial silicon wafer to ensure good thermal contact. The sacrificial wafer was mechanically clamped to the lower electrode,

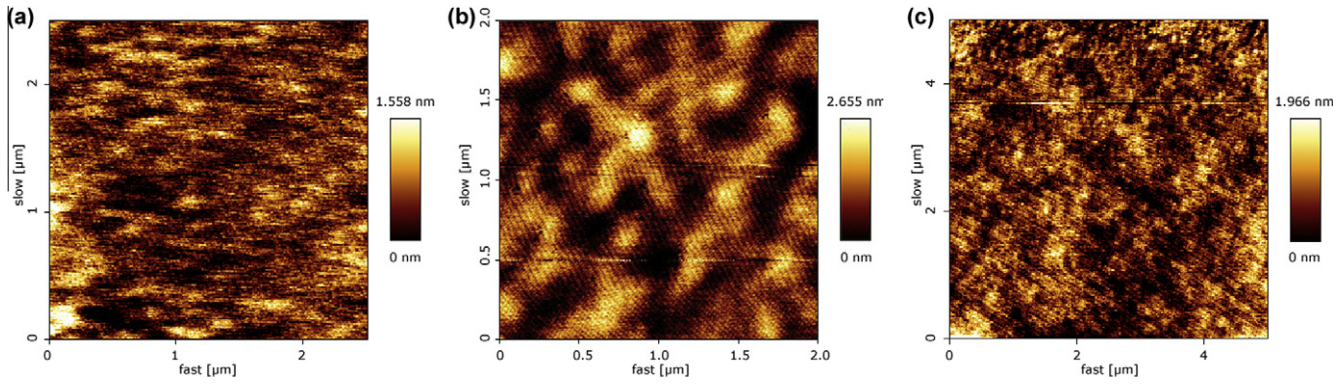

Fig. 2. AFM images of (a) reference sample of bare silicon, (b) an IM-HM11-01 film baked at 225 °C respectively, and (c) an IM-HM11-01 film baked at 375 °C.

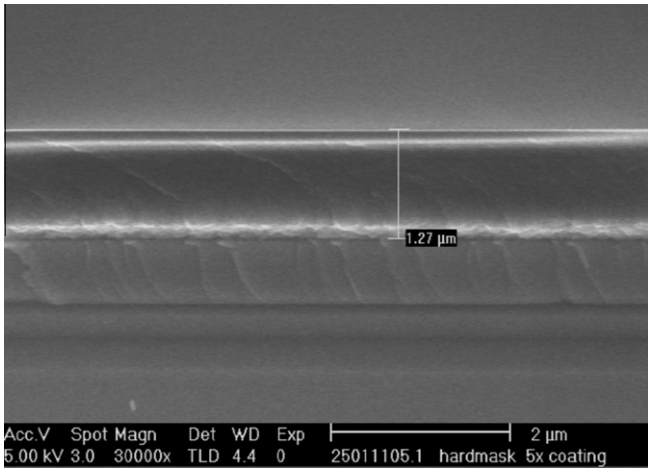

Fig. 3. SEM cross section of a SoC film of thickness 1.27 nm produced by spin coating five films consecutively with a heating step between each coating.

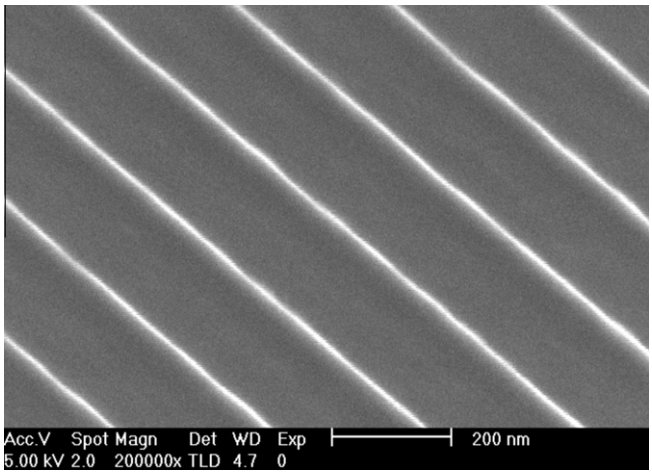

Fig. 4. Lines of 40 nm width transferred from a thin resist film into the silicon topcoat using an ICP etch. SEM image tilt is 45°.

which is equipped with helium backside pressure to ensure good thermal control of the sample during the etching process. The pattern was transferred into the silicon topcoat using a 20 s mixed mode SF_6/C_4F_8 ICP etch. SF_6 flow rate was 25 sccm and C_4F_8 flow rate 30 sccm. An RF power of 20 W and ICP power of 220 W were applied. Chamber pressure was 15 mT and the temperature was 1 °C. Fig. 4 shows 40 nm lines on a 200 nm pitch etched into the silicon on top of the SoC.

To transfer the pattern from the silicon to the IM-HM11-03 SoC an oxygen plasma etch was used. The selectivity of the silicon hardmask with respect to the carbon for oxygen plasma is extremely high, allowing transfer to thick carbon films. In order to minimize undercutting of the carbon, and maintain vertical sidewalls during the etch, a low chamber pressure was needed, and it was necessary to end the etch as soon as the etch depth reached the substrate or severe undercutting was seen at the SoC foot. Fig. 5 shows lines of 38 nm width on a 200 nm pitch etched through a 260 nm thick SoC film. Etch duration was 20 s with an O_2 flow rate of 15 sccm. RF power of 100 W and ICP power of 300 W were applied. Chamber pressure was 2 mT and the temperature was 1 °C.

The final step was to transfer the carbon hard mask pattern into the silicon substrate with another mixed mode SF_6/C_4F_8 ICP etch.

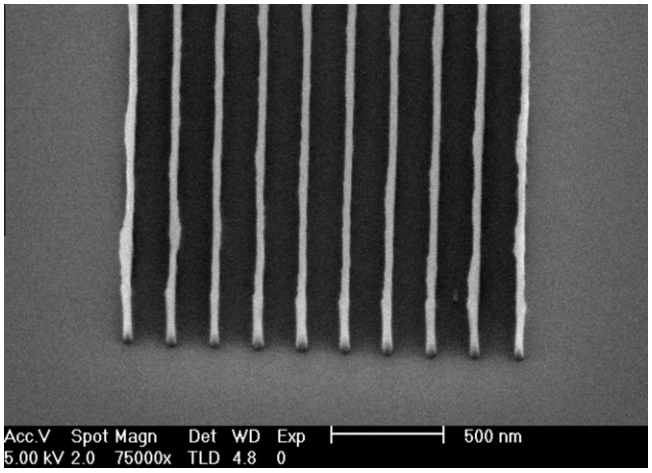

Fig. 5. SEM image showing lines of width 38 nm, with height 260 nm, transferred to the SoC by oxygen plasma etching. SEM image tilt is 44°.

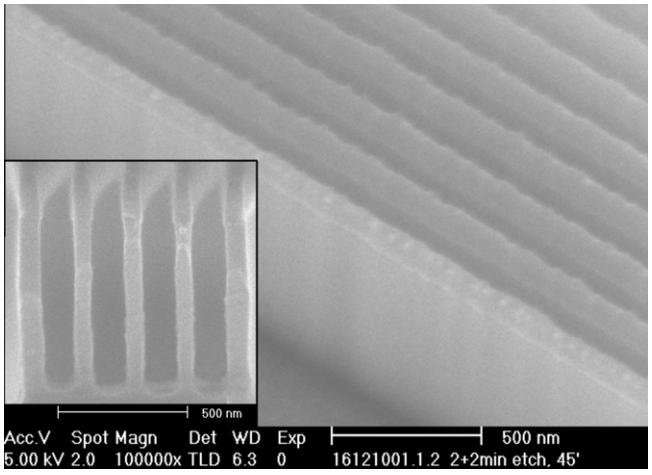

Fig. 6. Lines of 60 nm width and 700 nm height (aspect ratio 11.6:1) etched into the silicon substrate, using a mixed SF_6/C_4F_8 etch.

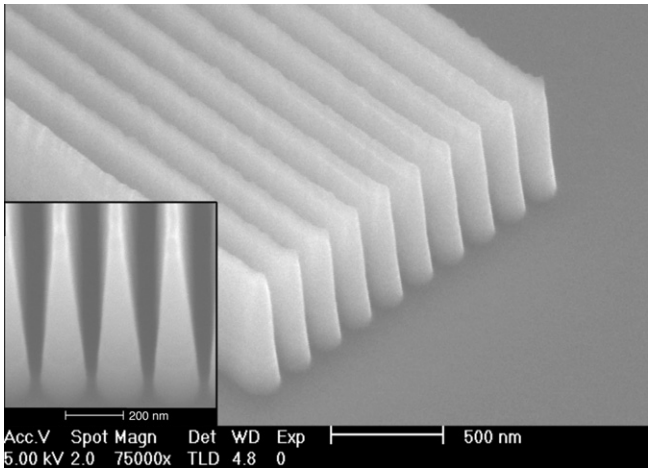

Fig. 7. Lines of 40 nm width and 718 nm height (aspect ratio 18:1) etched into the silicon substrate, using a mixed SF_6/C_4F_8 etch.

For semi-dense 60 nm lines silicon features with an aspect ratio of 11:1 were produced, as shown in Fig. 6, whilst for 40 nm linewidth features on a 200 nm pitch an aspect ratio of 18:1 (linewidth

measured at the top) were produced, as shown in Fig. 7. In both cases the mixed mode SF_6/C_4F_8 ICP etch parameters used were: SF_6 flow rate 20 sccm, C_4F_8 flow rate 30 sccm, RF power 20 W, ICP power 220 W. Chamber pressure was 15 mT. It can be seen from the inserts to Figs. 6 and 7 that the sidewall verticality is significantly degraded for the 40 nm features. Apart from the feature size the primary difference was that Fig. 6 was etched at 5 °C, whilst Fig. 7 was etched at 1 °C. Further optimization of the parameters for the 40 nm etch is required.

3. Conclusions

In summary, initial work on the development of a fullerene-derivative based spin-on-carbon material, aimed at increasing the achievable aspect ratio for sub-100 nm etching, has been presented. Films rich in aromatic carbon, from 20 to 325 nm in thickness, have been prepared by spin coating. A post-spin bake step renders the material insoluble in common organic solvents enabling further spin coating, and a multilayer carbon film of 1270 nm thickness has been prepared. Using a sputter coated thin silicon topcoat and a thin (30–100 nm) photoresist film, patterns with a linewidth of 40 nm have been transferred to the carbon layer with good sidewall verticality. Preliminary results of etching from the SoC pattern to the silicon substrate have shown 60 nm features etched with an aspect ratio in excess of 11:1. Smaller features have also successfully been transferred from the SoC to the substrate, but further work is required to optimize the sidewall angle. Using a suitable formulation of the fullerene SoC, the activation temperature for hardening can be as low at 190 °C – compatible with other microfabrication processes. Unlike current CVD approaches to the preparation of multilayer etch stacks the application process is simple, quick and does not require expensive deposition equipment. In comparison to polymers used in other SoC approaches fullerene is inherently low in hydrogen content, which has been shown to be key to reducing feature 'wiggling' as pattern halfpitch decreases [10]. The etch durability of fullerene based resists, described elsewhere [3], together with the high fidelity transfer of 40 nm patterns to the SoC layer suggest that aspect ratios in excess of 30:1 at feature sizes of 40 nm or less may be achievable.

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